Curriculum Vitae

Tatjana Nikolic

November 1, 2004.

A. PERSONAL DATA

Birth and Place date:	October 30, 1974, Lebane, Serbia and Montenegro
Home Address:	Mokranjceva 85/23, 18000 Nis, Serbia and Montenegro
Home Phone:	+381 18 530-110
Work Address:	Faculty of Electronic Engineering, Beogradska 14, P.O. Box 73, 18000 Nis, Serbia and Montenegro
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B. EDUCATIONAL HISTORY

April 2001 — University of Nis, Faculty of Electronic Engineering
Nis, Serbia and Montenegro
Dipl. Ing. in Electronics and Communications (5 years degree)
Diploma work: "GPS-38 receiver for global positioning"
GPA: 8.83/10.00

2002 - — University of Nis, Faculty of Electronic Engineering
Nis, Serbia and Montenegro
Study for master degree in Electronics (in progress)
Thesis: "Combinational and sequential self-checking circuits design based on VHDL"

C. PROFESSIONAL POSITIONS

2001 - University of Nis, Faculty of Electronic Engineering, Nis, Serbia and Montenegro

Position: ***Teaching Assistant****. Department of Electronics.*

Duties: Lectured and counseled students in three separate courses: "Microprocessors and microcomputers", "Microprocessor Systems" and "Electronics I".

Research: Microprocessor systems design and programming, VLSI ICs design, fault-tolerant systems, wireless sensor networks

D. MAIN RESEARCH PROJECTS

2002 - 2004 *Project name:* Ultrasonic Flowmeter for liquid meassurement
Financial support: Serbian Ministry of Science and Technology

E. REFERENCES (2001 - 2004)

Journal Papers

[1] G. Lj. Djordjevic, M. K. Stojcev, **T. R. Stankovic**, "Approach to partially self-checking combinational circuits design", *Microelectronics Journal* – accepted for publication

[2] M. K. Stojcev, G. Lj. Djordjevic, **T. R. Stankovic**, "Implementation of self-checking two-level combinational logic on FPGA and CPLD circuits", *Microelectronics Reliability*, Vol. 44, Issue 1, Elsevier, January 2004, pp. 173-178.

[3] **T. R. Stankovic**, M. K. Stojcev, G. Lj. Djordjevic, , "On VHDL Synthesis of Self-Checking Two-Level Combinational Circuits", *Facta Universitatis* (Nis), *Series: Electronics and Energetics,* Vol. 17, No. 1, April 2004, pp. 69-80.

[4] **Tatjana R. Stankovic**, Mile K. Stojcev, "*Implementation of Totally Self-checking Combinational Logic on FPGA and CPLD Circuits Using VHDL Descriptions* ", Cyprus Computer Society, Vol. 5, No. 5, June, 2003, pp. 40-44

[5] **Tatjana R. Stankovic**, Mile K. Stojcev, Goran Lj. Djordjevic, "*Design of Totally Self-Checking Combinational Circuits Based on VHDL Description*", ETF Journal of Electrical Engineering, Vol. 12, No. 1, May 2004, pp. 153 –161

Conference Papers

[1] M. K. Stojcev, G. Lj. Djordjevic, **T. R. Stankovic**, "VHDL-Based Design of FSM with Concurrent Error Detection Capability", *Proc. 24th International Conference on Microelectronics (MIEL 2004)*, Vol. 2, Niš, Serbia and Montenegro, May, 2004, pp. 759-762.

[2] M. Stojcev, **T. Stankovic**, P. Krtolica, "Lab Practicing in Studying the Assembly Languages and Computer Architectures", *Proceedings of Workshops on Computer Science Education*, Bitola, Macedonia, January, 2004, pp. 65-70

[3] **T. R. Stankovic**, M. K. Stojcev, G. Lj. Djordjevic, "Design Of Self-Checking Combinational Circuits", *6th International Conference on Telecommunications in Modern Satellite*, *TELSIKS 2003*, Niš, Serbia and Montenegro, October 1-3, 2003, pp. 763-768.

[4] **T. R. Stankovic**, M. K. Stojcev, G. Lj. Djordjevic, "On VHDL synthesis of self-checking two-level combinational circuits", *Third Triennial International Conference on Applied Automatic Systems*, Ohrid, Republic of Macedonia, September 18-20, 2003, pp. 225-230.

[5] **Tatjana R. Stanković**, Mile K. Stojcev, Goran Lj. Djordjević, "Design of totally

self-checking combinational circuits based on VHDL description", *Proc. XLVII Conference ETRAN 2003*, Herceg Novi, Serbia and Montenegro, June 2003, pp. 39-42

[6] **T. Stankovic**, M. Stojcev, "Parity Error Detection in Transceiver Circuit", Proc. IV simpozijum Industrijska elektronika INDEL -2002, Banja Luka, November 2002, pp. 67-73

[7] M. Stojcev, **T. Stankovic**, "Parity Error Detection in Embedded System", *28. naučno stručni skup "HIPNEF 2002", Zbornik radova,* Vrnjacka Banja, October 2002, pp. 215-220

[8] M. Stojcev, **T. Stankovic**, "Parity error detection in embedded system", *Second International Conference on Informatics and Information Technology*, *CiiT 2001*, Molika, December 20-23, 2001, pp. 293-307