Curriculum Vitae

Mile Stojcev

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A. PERSONAL DATA

Birth date and Place:	May 20, 1946, Bitola, Macedonia
Home Address:	Sumatovacka 9, 18000 Nis, Serbia and Montenegro
Home Phone:	+381 18 251-978
Work Address:	Faculty of Electronic Engineering, Beogradska 14, P.O. Box 73, 18000 Nis, Serbia and Montenegro
Work Phone:	+381 18 529-660
E-mail:	stojcev@elfak.ni.ac.yu

B. EDUCATIONAL HISTORY

June 1970 — University of Nis, Faculty of Electronic Engineering
Nis, Serbia and Montenegro
Dipl. Ing. in Computer Science (5 years degree)

March 1977 — University of Nis, Faculty of Electronic Engineering
Nis, Serbia and Montenegro
M.S.E. in EE and TC,
Thesis: "Sound transmission during horizontal blanking period"

July 1982 — University of Nis, Faculty of Electronic Engineering
Nis, Serbia and Montenegro
Ph.D. in CE and EE,
Dissertation: "Contribution in displaying of alpha numeric and graphical symbol on the CRT"

C. PROFESSIONAL POSITIONS

1978 - 1982 — University of Nis, Faculty of Electronic Engineering, Nis, Serbia and Montenegro

Position: ***Teaching Assistant****. Department of Electronics.*

Duties: Lectured and counseled students in three separate courses: “Television”, “Digital Electronic Circuits”, and “Electronic I”.

1982 - 1987 — University of Nis, Faculty of Electronic Engineering, Nis, Serbia and Montenegro

Position: ***Assistant Professor****. Department of Electronics*

Duties: Taught three separate courses: “Design of Microprocessor

Systems", "Television" and "Computer Input Output Subsystems". Formulated course structure and requirements, lectured and administrated all grades.

Research: Microprocessor systems, embedded systems, distributed architectures and parallel processing.

1987 - 1992 University of Nis**,** Faculty of Electronic Engineering, Nis, Serbia and Montenegro

*Position: **Associate Professor**. Department of Electronics*

Duties: Teach three separate courses: "Design of Microprocessor Systems", "Design of Microcomputer Systems" and "Parallel and Distributed Computer Systems". Formulated course structure and requirements, lectured and administrated all grades.
Research: Parallel and distributed systems and algorithms, embedded systems, fault-tolerant systems, microprocessor and microcomputer systems.

1992 - Present University of Nis**,** Faculty of Electronic Engineering, Nis, Serbia and Montenegro

*Position: **Full Professor**. Department of Electronics*

Duties: Teach two separate courses: "Design of Microprocessor Systems", and "Design of Microcomputer Systems". Formulated course structure and requirements, lectured and administrated all grades.

Research: Parallel computer systems, microcomputer systems, embedded systems, fault-tolerant systems, wireless sensor networks.

D. PARTICIPATION IN RESEARCH PROJECTS

1991 – 1995 *Project name:* Computing
Financial support: Serbian Ministry of Science and Technology

1991 – 1994 *Project name:* Parallel and Distributed Computing
Financial support: Serbian Ministry of Science and Technology

1995 – 1998 *Project name:* Parallel and Distributed Computing in Data Acquisition Systems
Financial support: Serbian Ministry of Science and Technology

1996 – 2000 *Project name:* Computing
Financial support: Serbian Ministry of Science and Technology

2002 - 2004 *Project name:* Ultrasonic Flowmeter for liquid meassurement
Financial support: Serbian Ministry of Science and Technology

E. REFERENCES (1999 - 2004)

Journal Papers

[1] G. Lj. Djordjevic, **M. K. Stojcev**, T. R. Stankovic, "Approach to partially self-checking combinational circuits design", *Microelectronics Journal* – accepted for publication

[2] M. D. Krstic, **M. K. Stojcev**, G. Lj. Djordjevic, I. D. Andrejic, "A Mid-Value Select Voter", *Microelectronics Reliability* – accepted for publication.

[3] **Mile K. Stojcev**, Teufik Tokic, and Ivan Milentijevic, "The Limits of Semiconductor Technology and Oncoming Challenges in Computer Microarchitectures and Architectures", *Facta Universitatis*. Ser. Elec. Energ., Vol 17, December 2004, pp. 285-312

[4] Goran S. Jovanovic, **Mile K. Stojcev**, "Pulsewidth Control Loop as a Duty Cycle Corrector" *Serbian Journal of Electrical Engineering*, Vol. 1, No. 2, June 2004, pp. 215-226

[5] Tatjana R. Stankovic, **Mile K. Stojcev**, Goran Lj. Djordjevic, "Design of Totally Self-Checking Combinational Circuits Based on VHDL Description", *ETF Journal of Electrical Engineering*, Vol. 12, No. 1, May 2004, pp. 153 –161

[6] T. R. Stankovic, **M. K. Stojcev**, G. Lj. Djordjevic, , "On VHDL Synthesis of Self-Checking Two-Level Combinational Circuits", *Facta Universitatis* (Nis), *Series: Electronics and Energetics,* Vol. 17, No. 1, April 2004, pp. 69-80.

[7] **M. K. Stojcev**, G. Lj. Djordjevic, T. R. Stankovic, "Implementation of self-checking two-level combinational logic on FPGA and CPLD circuits", *Microelectronics Reliability*, Vol. 44, Issue 1, Elsevier, January 2004, pp. 173-178.

[8] B. D. Petrovic, **M. K. Stojcev**, "Phase Measurement System based on Embedded Microcomputer", *Facta Universitatis, series Mechanical Engineering*, University of Niš, Vol.1, No.10, 2003., pp. 1355-1368

[9] **M. Stojcev**, I.Z. Milentijevic, D. Kehagias, R. Drechsler, M. Gusev, "Computer Architecture Core of Knowledge for Computer Science Studies", *Cyprus Computer Society Journal*, Vol. 5., No. 4, March 2003, pp. 39-42

[10] Tatjana R. Stanković, **Mile K. Stojcev**, "Implementation of Totally Self-checking Combinational Logic on FPGA and CPLD Circuits Using VHDL Descriptions", *Cyprus Computer Society Journal*, Vol. 5, No. 5, June, 2003, pp. 40-44

[11] Goran S. Jovanović, **Mile K. Stojcev**, "Voltage Controlled Delay Line for Digital Signal", *Facta Universitatis, Series: Electronics and Energetic*, Vol 16. No. 2, pp. 215-232, August 2003.

[12] **M.K. Stojcev**, G.Lj. Djordjevic, M.D. Krstic, "A hardware mid-value select voter architecture", *Microelectronics Journal,* Vol. 32, No. 2, (2001) pp. 149-162.

[13] E. I. Milovanovic, **M. K. Stojcev**, N. M. Novakovic, I. Z. Milovanovic, T. I. Tokic, "Matrix-vector multiplication on fixed-size linear systolic array"*, Comput. Math. Appl*., 40 (2000), 1189-1203.

[14] I. Z. Milovanovic, T. I. Tokic, E. I. Milovanovic**, M. K. Stojčev**, "Determining

number of processing elements in systolic arrays”, *Facta Univ. Ser. Math. Inform*., 15 (1) (2000), 123-132.

[15] T. I. Tokić, E. I. Milovanović**,** N. M. Novaković, I. Z. Milovanović, **M. K. Stojčev**, “Matrix multiplication on non-planar systolic arrays”, *Facta Univ. Ser. Electr. Energet*., 13 (2) (2000), 157-165.

[16] **M.K. Stojcev**, G.Lj. Djordjevic, E.I. Milovanovic, I.Z. Milovanovic, “Data reordering converter: an interface block in a linear chain of processing arrays”, *Microelectronics Journal*, Vol. 31, No. 1 (2000) pp. 23-37.

[17] **M.K. Stojcev**, M. Krstic, G.Lj. Djordjevic, I. Andrejic, “Hardware voter architecture with implemented Hamming code logic”, *Electronics*, Vol. 4, No. 2, Dec. 2000., pp. 36-40.

Conference Papers

[1] **M. K. Stojcev**, G. Lj. Djordjevic, T. R. Stankovic, “VHDL-Based Design of FSM with Concurrent Error Detection Capability”, *Proc. 24th International Conference on Microelectronics (MIEL 2004)*, Vol. 2, Niš, Serbia and Montenegro, May, 2004, pp. 759-762.

[2] Goran S. Jovanovic, **Mile K. Stojcev**, “Voltage Controlled Active Delay Element”, *ICEST 2004***,** Bitola**,** June 2004.

[3] T. R. Stankovic, **M. K. Stojcev**, G. Lj. Djordjevic, “Design Of Self-Checking Combinational Circuits”, *6th International Conference on Telecommunications in Modern Satellite*, *TELSIKS 2003*, Niš, Serbia and Montenegro, October 1-3, 2003, pp. 763-768.

[4] Goran S. Jovanović, **Mile K. Stojčev**, “High Resolution Time to Digital Converter”, XLVII ETRAN, vol. I, pp.108-111, Herceg Novi, Jun 2003. (in Serbian)

[5] T. R. Stankovic, **M. K. Stojcev**, G. Lj. Djordjevic, “On VHDL synthesis of self-checking two-level combinational circuits”, *Third Triennial International Conference on Applied Automatic Systems*, Ohrid, Republic of Macedonia, September 18-20, 2003, pp. 225-230.

[6] G. S. Jovanovic, **M. K. Stojcev**, G. Lj. Djordjevic, B. D. Petrovic, “High Resolution Time-to-Digital Converter Utilizing Dual-Slope Principle”, *6th International Conference on Telecommunications in Modern Satellite, TELSIKS 2003*, Niš, Serbia and Montenegro, October 1-3, 2003, pp. 139-142.

[7] Goran S. Jovanovic, **Mile K. Stojcev**, “High Resolution Time-to-Digital Converter”, *ICEST 2003*, pp. 402-406, Sofia, October 2003.

[8] Goran Jovanovic, **Mile Stojcev**, “Low-Power Design trough Multi-Phase and Multi–Frequency Clock”, *ICEST 2002*, Volume 1, pp.77-80, Niš, Oktobar 2002

[9] **Mile Stojcev**, Goran Jovanović, “Design for Low-Power Using Multi-Phase and

Multi-Frequency Clocking", 3rd *Int. Conf. CiiT 2002*, vol. 1, pp. 31-41, Molika, December 2002.

[10] **Mile K. Stojčev**, Goran S. Jovanović, "Architecture of Voltage Controlled Delay Line for Digital Signal in DLL", *XLVI ETRAN*, vol. I, pp.21-24, Banja Vrućica – Teslić, Jun 2002. (in Serbian)

[11] Goran S. Jovanović, **Mile K. Stojčev**, "Voltage Controlled Delay Line for Digital Signal", XLVI ETRAN, vol. I, pp.39-42, Banja Vrućica – Teslić, Jun 2002. (in Serbian)

[12] **M. Stojcev**, G. Djordjevic, M. Krstic, I. Andrejic, "HMVSA – A Hardware Mid-Value Select Voter Architecture", in *Proc. of ETAI 2000, Ohrid, Macedonia*, 2000, pp. 54-59.