Curriculum Vitae

Goran Djordjevic

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A. PERSONAL DATA

Birth date and Place:	June 15, 1964, Nis, Serbia and Montenegro
Home Address:	Juznomoravskih brigada 7, 18000 Nis, Serbia and Montenegro
Home Phone:	+381 18 222-728
Office Address:	Faculty of Electronic Engineering, A. Medvedeva 14, P.O. Box 73, 18000 Nis, Serbia and Montenegro
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B. EDUCATIONAL HISTORY

June 1989	University of Nis, Faculty of Electronic Engineering Nis, Serbia and Montenegro **Dipl. Ing.** in Computer Science (5 years degree)
June 1994	University of Nis, Faculty of Electronic Engineering Nis, Serbia and Montenegro **M.Sc. in Computer Science**, *Thesis*: "Interprocessor communication interface for message-passing via shared memory modules"
December 1998	University of Nis, Faculty of Electronic Engineering Nis, Serbia and Montenegro **Ph.D.** in Computer Science, *Dissertation*: "Multiprocessor scheduling algorithms based on chaining technique"

C. PROFESSIONAL POSITIONS

1990 - 1995	University of Nis, Faculty of Electronic Engineering, Nis, Serbia and Montenegro *Position:* ***Junior Teaching Assistant.*** *Department of Electronics.* *Duties:* Lectured and counseled students in three separate courses: "Electronics II", "Digital Electronic Circuits", and "Electronic System Design".
1995 - 1999	University of Nis**,** Faculty of Electronic Engineering, Nis, Serbia and Montenegro

Position: ***Research and Teaching Assistant.*** *Department of Electronics.*

Duties: Lectured and counseled students in two separate courses: "Digital electronics", and "Electronic System Design". Composed exams and term paper assignments, grade all written work.

Research: Parallel processing architectures, digital hardware design, VLSI architectures.

1999 - 2004 University of Nis, Faculty of Electronic Engineering, Nis, Serbia and Montenegro

Position: ***Assistant Professor.*** *Department of Electronics*

Duties: Taught two separate courses: "Design of Microprocessor Systems", and "Architecture of Microsystems". Formulated course structure and requirements, lectured and administrated all grades.

Research: Embedded systems, distributed architectures, VLSI structures for DSP.

2004 - 2009 University of Nis**,** Faculty of Electronic Engineering, Nis, Serbia

Position: ***Associate Professor.*** *Department of Electronics*

Duties: Teach two separate courses: "Design of Microprocessor Systems", and "Architecture of Microsystems". Formulated course structure and requirements, lectured and administrated all grades.

Research: Embedded systems, fault-tolerant systems, wireless sensor networks.

2009 - Present University of Nis**,** Faculty of Electronic Engineering, Nis, Serbia

Position: ***Full Professor.*** *Department of Electronics*

Duties: Teach several separate courses in the areas of embedded systems and computer networks. Formulated course structure and requirements.

Research: Embedded systems, wireless sensor networks.

D. PARTICIPATION IN RESEARCH PROJECTS

1991 – 1995 *Project name:* Parallel and distributed systems
Financial support: Serbian Ministry of Science and Technology

1996 – 2000 *Project name:* Parallel and distributed systems
Financial support: Serbian Ministry of Science and Technology

2002 - 2004 *Project name:* Ultrasonic Flowmeter for liquid meassurement
Financial support: Serbian Ministry of Science and Technology

2004 - 2008 *Project name:* Wireless Sensor Networks
Financial support: Serbian Ministry of Science and Technology

E. REFERENCES

a) Papers published in international journals

a1. M. D. Krstic, M. K. Stojcev, **G. Lj. Djordjevic**, I. D. Andrejic, „*A Mid-Value Select Voter*“ , Microelectronics Reliability, Elsevier Ltd, Vol. 45, No. 3-4, pp.733-738, March-April 2005. ISSN**:** 0026-2714. http://dx.doi.org/10.1016/j.microrel.2004.07.006 **(M22)**

a2. **G. Lj. Djordjevic**, M. K. Stojcev, T. R. Stankovic, „*Approach to partially self-checking combinational circuit design*“, Microelectronics Journal, Elsevier Ltd, Vol. 35, No. 12, pp. 945-952, December 2004. ISSN: 0026-2692. http://dx.doi.org/10.1016/j.mejo.2004.07.007 **(M23)**

a3. M. K. Stojčev, **G. Lj. Djordjevic**, T. R. Stanković, "*Implementation of self-checking two-level combinational logic on FPGA and CPLD circuits*", Microelectronics Reliability, Vol. 44, No. 1, Elsevier Inc, pp. 173-178, January 2004. ISSN**:** 0026-2714 http://dx.doi.org/10.1016/S0026-2714(03)00377-9 **(M23)**

a4. M. K. Stojcev, **G. Lj. Djordjevic**, M.D. Krstic, "*A hardware mid-value select voter architecture*", Microelectronics Journal, Vol. 32, No. 2, pp. 149-162, 2001. ISSN: 0026-2692. http://dx.doi.org/10.1016/S0026-2692(00)00114-2 **(M23)**

a5. B.Vasic, **G. Lj. Djordjevic**, M.Tosic, "*Loose Composite Constraint Codes and Their Application in DVD*", IEEE Journal of Selected Area in Communications, Vol. 19, No. 4, pp. 765 –773, April 2001. ISSN: 0733-8716. http://dx.doi.org/10.1109/49.920184 **(M21)**

a6. M. K. Stojcev, **G. Lj. Djordjevic**, E. I. Milovanovic, I. Z. Milovanovic, "*Data reordering converter: an interface block in a linear chain of processing arrays*", Microelectronics Journal, Elsevier Inc, Vol. 31, No. 1, pp. 23-37, 2000. ISSN: 0026-2692 http://dx.doi.org/10.1016/S0026-2692(99)00086-5 **(M23)**

a7. M. Tosic, M. Stojcev, D. Maksimovic, **G. Lj. Djordjevic**, "*The asynchronous counterflow pipeline bit-serial multiplier*", Journal of System Architecture, Elsevier B.V, Vol. 44, No. 12, pp. 985-1004, 1998. ISSN: 1383-7621. http://dx.doi.org/10.1016/S1383-7621(97)00046-5 **(M23)**

a8. **G. Lj. Djordjevic** and M. B. Tosic, "*A heuristic for scheduling task graphs with communication delays onto multiprocessors*", Parallel Computing, Elsevier Science B.V., Vol. 22, No. 9, pp. 1197-1214. 1996. ISSN: 0167-8191. http://dx.doi.org/10.1016/S0167-8191(96)00041-5 **(M22)**

a9. **G. Lj. Djordjevic**, M.B. Tosic, "*A compile-time scheduling heuristic for multiprocessor architectures*", The Computer Journal, Oxford University Press,Vol.39, No.8, pp 663-674, 1996. ISSN: 0010-4620. http://dx.doi.org/10.1093/comjnl/39.8.663. **(M23)**

a10. **G. Lj. Djordjevic**, M.K. Stojcev, "*An interprocessor communication interface for message passing via shared memory modules - design and performances*", Computers and Artificial Intelligence, Slovak Academic Press Ltd, Vol. 15, No. 1, pp. 1-33., 1996, ISSN 1335-9150. http://www.cai.sk/ **(M23)**

b) Papers published in national journals

b1. Andrija S. Velimirović, **Goran Lj. Djordjević**, Maja M. Velimirović, and Milica D. Jovanović: "*A Fuzzy Set-Based Approach to Range-Free Localization in Wireless Sensor Networks*", Facta Univ. Ser.: Elec. Energ., vol. 23, No. 2, August 2010, pp. 227-244. YU ISSN 0353-3670. **(M51)**

b2. T. R. Stankovic, M. K. Stojcev, **G. Lj. Djordjevic**, *"Design of Totally Self-Checking Combinational Circuits Based on VHDL Description"*, ETF Journal of Electrical Engineering, A Publication of the EE Department, University of Montenegro, Vol. 12, No. 1, pp. 153 –161, May 2004. YU ISSN 0353-5207. **(M51)**

b3. T. R. Stankovic, M. K. Stojcev, **G. Lj. Djordjevic**, *"On VHDL Synthesis of Self-Checking Two-Level Combinational Circuits"*, Facta Universitatis (Nis), Series: Electronics and Energetics, Vol. 17, No. 1, pp. 69-80, April 2004. YU ISSN 0353-3670. http://factaee.elfak.ni.ac.yu/fu2k41/7ts.html **(M51)**

b4. B.Vasic, **G.Djordjevic**, M.Tosic, "*EFM++ an Efficient Coding Format For DVD*", Facta Universitatis (Nis), Series: Electronics and Energetics, Vol. 13, No. 3, December 2000, 263—296. YU ISSN 0353-3670. http://factaee.elfak.ni.ac.yu/fu2k03/fu01.html **(M51)**

b5. M. K. Stojcev, M. Krstic, **G. Lj. Djordjevic**, I. Andrejic, "*Hardware voter architecture with implemented Hamming code logic*", Electronics, University of Banja Luka, YU ISSN: 1450-5843, Vol. 4, No. 2, Dec. 2000., pp. 36-40. YU ISSN 1450-5843. **(M51)**

c) Conference papers

c1. Milica D. Jovanovic, **Goran Lj. Djordjevic,** "CT-MAC: Energy-Efficient Contention-based MAC Protocol for Wireless Sensor Networks", XLV International Scientific Conference on Information, Communication and Energy Systems and Technologies, ICEST 2010, 23-26 June, 2010, Ohrid, Macedonia, Vol. 1, pp. 19-22. **(M33)**

c2. T. R. Nikolic, **G. Lj. Djordjevic**, and M. K. Stojcev, "*Simultaneous Data Transfers over Peripheral Bus Using CDMA Technique*", *Proc. 26th International Conference on Microelectronics (MIEL 2008)*, Niš, Serbia, 11-14 May, 2008, pp. 437-440. **(M33)**

c3. T. R. Nikolic, **G. Lj. Djordjevic**, and M. K. Stojcev, "*Low Power Application Specific Processing Element*", XLII International Scientific Conference on Information, Communication and Energy Systems and Technologies, ICEST 2007, ISBN: 9989-786-06-2, vol. 1, pp. 135-138, Ohrid, 24-27 June 2007. **(M33)**

c4. M. D. Jovanovic, **G. Lj. Djordjevic**, *TFMAC: Multi-channel MAC Protocol for Wireless Sensor Networks*, in Proc. of 8-th International Conference on Telecommunications in Modern Satellite, Cable and Broadcasting Services (TELSIKS), Nis, Serbia, September 2007, pp. 23-26. **(M33)**

c5. D. B. Stankovic, M. K. Stojcev, and **G. Lj. Djordjevic**, *Power Reduction Technique for Successive-Approximation Analog-to-Digital Converters*, in Proc. of 8-th International Conference on Telecommunications in Modern Satellite, Cable and Broadcasting Services (TELSIKS), Nis, Serbia, September 2007, pp. 355-358. **(M33)**

c6. **G. Lj. Djordjevic**, T. R. Stankovic, M. K Stojcev, *Approach to Partially Self-Checking Finite State Machine Design*, Proc. 25th International Conference on Microelectronics (MIEL 2006), Belgrade, Serbia and Montenegro, Vol.2, 14-17 May, 2006, pp. 697-700. **(M33)**

c7. **G. Lj. Djordjevic**, T. R. Stankovic, M. K. Stojcev, *Concurrent Error Detection in FSMs Using Transition Checking Technique*, in Proc. of 7-th International Conference on Telecommunications in Modern Satellite, Cable and Broadcasting Services (TELSIKS) vol. 1, Nis, Serbia and Montenegro, September 2005, pp. 61-64. **(M33)**

c8. M. K. Stojcev, **G. Lj. Djordjevic**, T. R. Stankovic, *"VHDL-Based Design of FSM with Concurrent Error Detection Capability"*, Proc. 24th International Conference on

Microelectronics (MIEL 2004), Vol. 2, Niš, Serbia and Montenegro, May, 2004, pp. 759-762. **(M33)**

c9. T. R. Stankovic, M. K. Stojcev, **G. Lj. Djordjevic**, "*On VHDL synthesis of self-checking two-level combinational circuits*", Third Triennial International Conference on Applied Automatic Systems, Ohrid, Republic of Macedonia, September 18-20, 2003, pp. 225-230. **(M33)**

c10. G. S. Jovanovic, M. K. Stojcev, **G. Lj. Djordjevic**, B. D. Petrovic, "High Resolution Time-to-Digital Converter Utilizing Dual-Slope Principle", *6th International Conference on Telecommunications in Modern Satellite, TELSIKS 2003*, Niš, Serbia and Montenegro, October 1-3, 2003, pp. 139-142. **(M33)**

c11. M. Stojcev, **G. Djordjevic**, M. Krstic, I. Andrejic, "HMVSA – A Hardware Mid-Value Select Voter Architecture", in *Proc. of ETAI 2000, Ohrid, Macedonia*, 2000, pp. 54-59. **(M33)**

c12. **G. Lj. Djordjevic,** M. K. Stojcev, "A multistream RISC architecture for high-speed digital signal processing", *Proc. 3nt International Conference on Telecommunications in Modern Satellite, Cable and Broadcasting Services* (*TELSIKS*), Vol. 1, Nis, 1997, pp. 261-264. **(M33)**

c13. M. Tosic, M. Stojcev, **G. Lj. Djordjevic**, "Asynchronous controller for token-ring mutual exclusion: Delay-insensitive arbiter cell," *Proc. 21th International Conference on Microelectronics* (*MIEL*), Vol.2., Nis, 1997, pp. 819-822. **(M33)**

c14. M. K. Stojcev, M. Tosic, **G.Lj.Djordjevic**, "Asynchronous full-adder cells for digital signal processing", *Proc. 3nt International Conference on Telecommunications in Modern Satellite, Cable and Broadcasting Services* (*TELSIKS*), Vol. 1, Nis, 1997, pp. 255-260. **(M33)**

c15. M. Tosic, M. Stojcev, **G. Lj. Djordjevic**, "Asynchronous controller for token-ring mutual exclusion: Ring design," *Proc. 21th International Conference on Microelectronics* (*MIEL*), Vol.2., Nis, 1997, pp. 823-826. **(M33)**

d) Papers presented at national conferences

d1. T. R. Nikolic, **G. Lj. Djordjevic**, and M. K. Stojcev, "*Micro-power simple processing elemen*t", Proc. 8th National Conference with International Participation, ETAI 2007, Ohrid, 19 – 21. September 2007., CD ROM - E2-1. ISBN 978998921753X. **(M63)**

d2. D. B. Stankovic, M. K. Stojcev, **G. Lj. Djordjevic**, "*Smanjenje potrošnje energije kod A/D konvertora sa sukcesivnom aproksimacijom", Zbornik radova 50. konferencije za ETRAN, Beograd, 6-8. juna 2006. tom I, pp. 68-71*. **(M63)**

d3. D. B. Stankovic, M. D. Mitic, **G. Lj. Djordjevic**, *"VHDL opis konfigurabilnog mikrokontrolera za implementaciju na FPGA"*, 13th Telecommunications Forum Telfor 2005, 22-24. 11. 2005. Belgrade, Serbia and Montenegro, November 2005. http://www.telfor.rs/telfor2005/radovi/PEL-7.13.pdf **(M63)**

d4. T. R. Stankovic, M. K. Stojcev, **G. Lj. Djordjevic**, "Design of totally self-checking combinational circuits based on VHDL description", *XLVII Konferencija ETRAN 2003*, Zbornik radova, Herceg Novi, 8-13. jun, 2003, str. 39-42. **(M63)**

d5. M. Krstić, M. Stojčev, **G. Lj. Djordjević**, "Hardversko glasačka arhitektura bazirana na izboru srednje vrednosti", *Zbornik radova Konferencije ETRAN 2000*, sveska III, 2000, str. 91-95. **(M63)**

d6. **G. Lj. Djordjević**, M. Krstic, M. Stojcev, "Glasacka jedinica kod visoko-pouzdanih sistema za akviziciju podataka", *Zbornik radova Konferencije ETRAN 1999*, sveska I, 2000, str. 46-48. **(M63)**

d7. **G. Lj. Djordjević**, M.B. Tošić, "Aproksimacioni algoritam za statičko planiranje paralelnih programskih zadataka", *Zbornik radova XXXVIII Konferencije ETRAN 1994*, sveska III, Niš, 1994, str. 63-64. **(M63)**

d8. **G. Lj. Djordjević**, "Heuristički algoritam za statičko planiranje paralelnih programskih zadataka", *Zbornik radova XXXIX Konferencije ETRAN 1995*, Zlatibor, 1995, str.291-293. **(M63)**

d9. **G. Lj. Djordjević**, M. Stojčev, "Hardverska podrška implementaciji tehnike prenosa poruka kod multiprocesora sa deljivom memorijom", *Zbornik radova XXXVII Konferencije ETRAN 1993*, Beograd, 1993, str.197-202. **(M63)**

d10. **G. Lj. Djordjević**, M. Stojčev, "Interprocesorski komunikacioni interfejs baziran na FIFO baferima", *Zbornik radova XXXVII Konferencije ETRAN 1993*, Beograd, 1993, str.405-410. **(M63)**