Serijski komunikacioni interfejs SCI

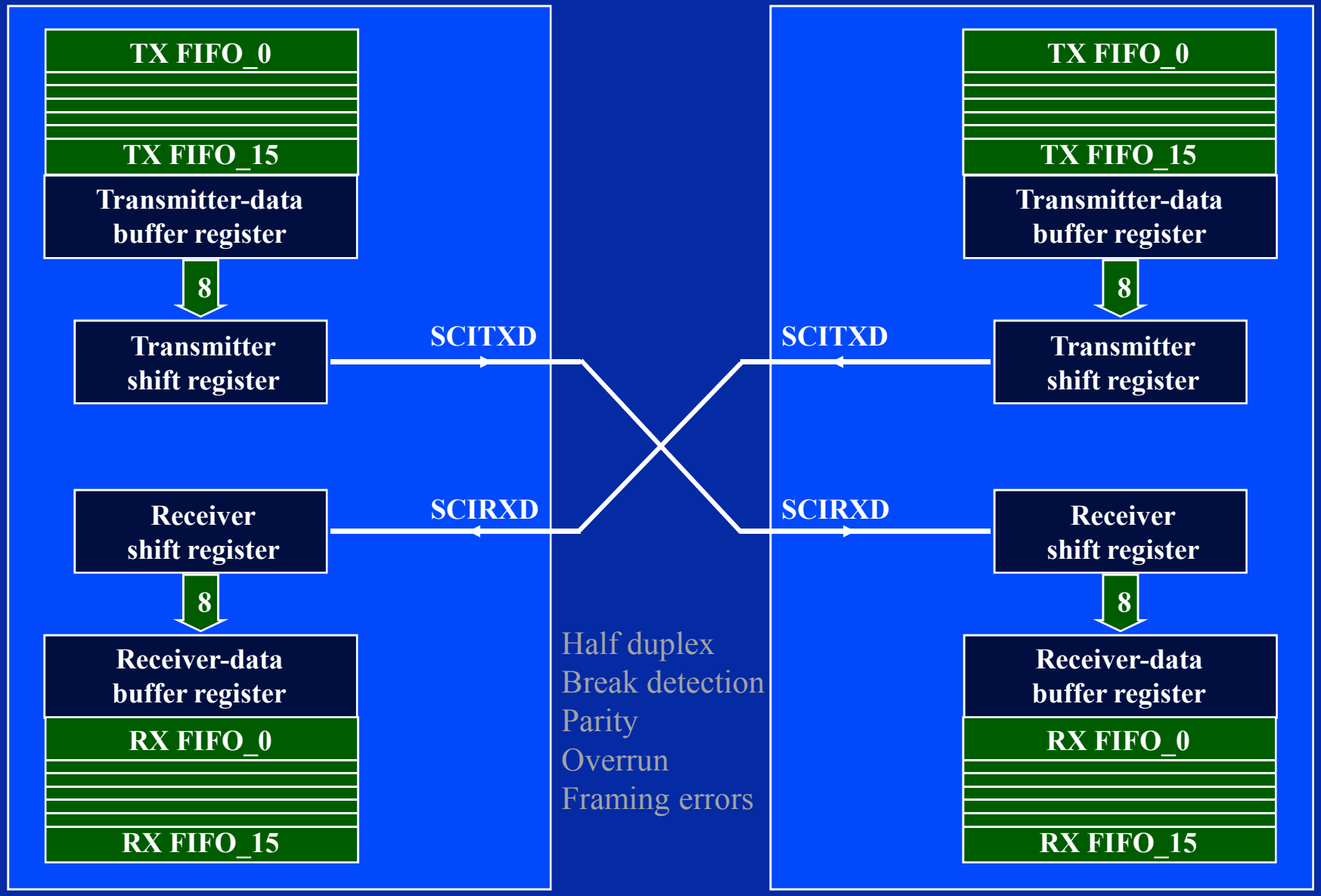
Serial Communication Interface

32-Bit-Digital Signal Controller
TMS320F2833x

Texas Instruments Incorporated

SCI Pin Connections

(Full Duplex)



SCI Data Format

Character
Frame
Block

NRZ (non-return to zero) format

Bit prisutan samo u *Address-bit* režimu

Communications Control Register (ScixRegs.SCICCR)

7	6	5	4	3	2	1	0
Stop Bits	Even/Odd Parity	Parity Enable	Loopback Enable	Addr/Idle Mode	SCI Char2	SCI Char1	SCI Char0

0 = 1 Stop bit
1 = 2 Stop bits

0 = Odd
1 = Even

0 = Disabled
1 = Enabled

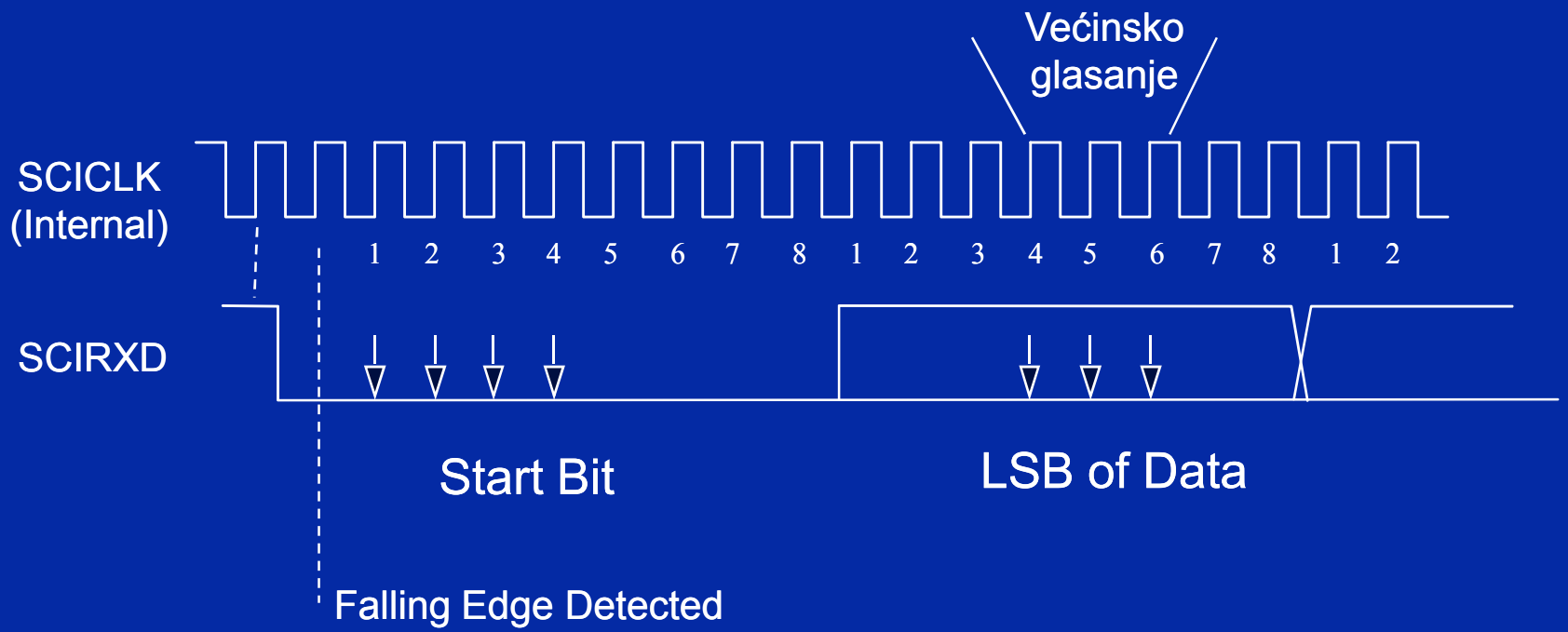
0 = Disabled
1 = Enabled

0 = Idle-line mode
1 = Addr-bit mode

broj bitova u karakteru
(binary + 1)
110b == 7 bitova

SCI Data Timing

- Start bit važeći ako se nula detektuje u 4 uzastopne SCICLK periode nakon detekcije opadajuće ivice – *falling edge*
- Većinsko glasanje na 4, 5, i 6 SCICLK ciklusu



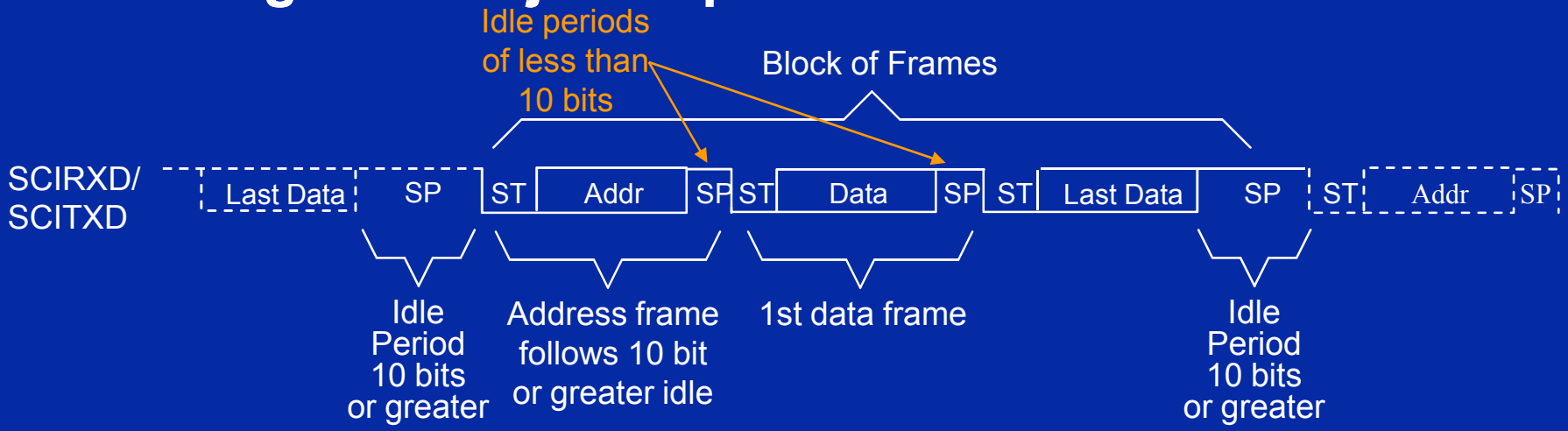
Napomena: 8 SCICLK perioda po jednom bitu podatka

Višeprocesorski *Wake-Up* režimi

- **Omogućava povezivanje većeg broja procesora na magistrali ali razmenu podataka samo između dva procesora**
- ***Idle-line* or *Address-bit* režim rada**
- **Sekvence slanja podataka**
  1. Svi prijemnici postavljaju SLEEP = 1, čime je zabranjen RXINT osim kada se primi adresni frejm (ADDR/DATA = 1)
  2. Svi prenosi podataka započinu adresnim frejmom
  3. Prijem adresnog frejma privremeno budi sve SCI na magistrali
  4. CPU upoređuje primljenu adresu sa sopstvenom
  5. Prihvata sledeće podatke samo ako se adrese slažu

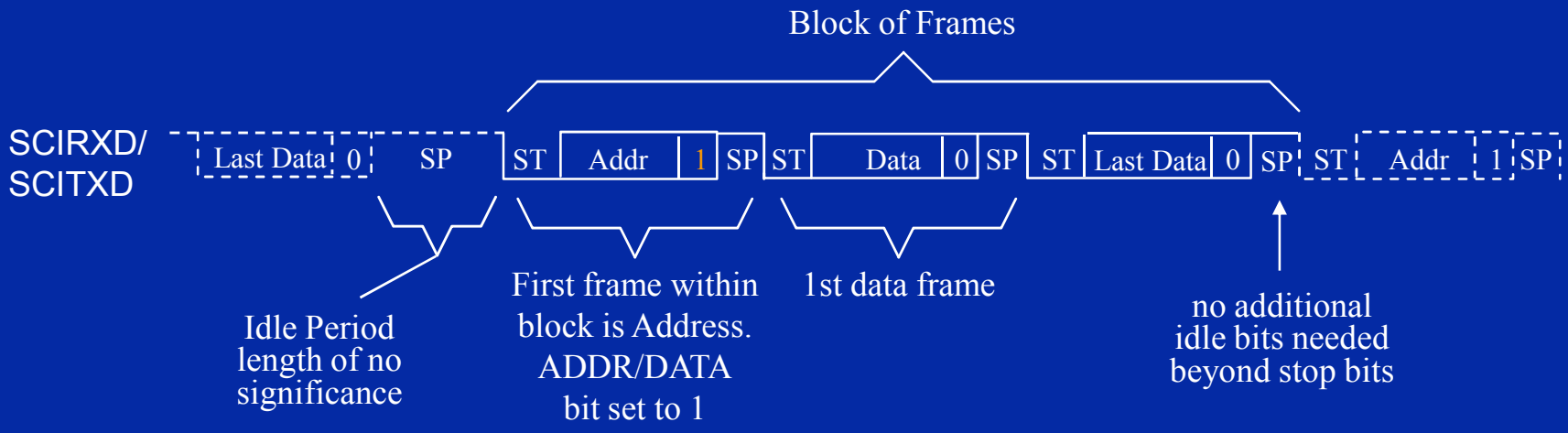
Idle-Line Wake-Up režim

- Idle time odvaja blokove frejmova
- Prijemnik se budi zadnjom ivicom nakon 10 ili više perioda u toku kojih je linija SCIRXD bila na visokom nivou
- Dva načina adresiranja
  - Softversko kašnjenje od 10 i više bitova
  - Postavljanje bita TXWAKE za automatsko generisanje idle perioda od 11 taktova



Address-Bit Wake-Up Mode

- Svaki frejm sadrži dodatni adresni bit
- Prijemnik se budi kada detektuje postavljeni adresni bit
- Automatsko postavljanje Addr/Data bita u frajmu postavljanjem TXWAKE = 1 pre upisa adrese u SCITXBUF



SCI Summary

- Asinhroni komunikacioni format
- 65,000+ različitih programabilnih brzina
- Dva *wake-up* multiprocesorska režima
  - Idle-line wake-up & Address-bit wake-up
- Programabilni format podataka
  - 1 to 8 bit data word length
  - 1 or 2 stop bits
  - even/odd/no parity
- Markeri detekcije grešaka
  - Parity error; Framing error; Overrun error; Break detection
- FIFO-baferi za prijem i predaju
- Posebni prekidi za prijem i predaju
- 28335 poseduje dva kanala SCI-A i SCI-B

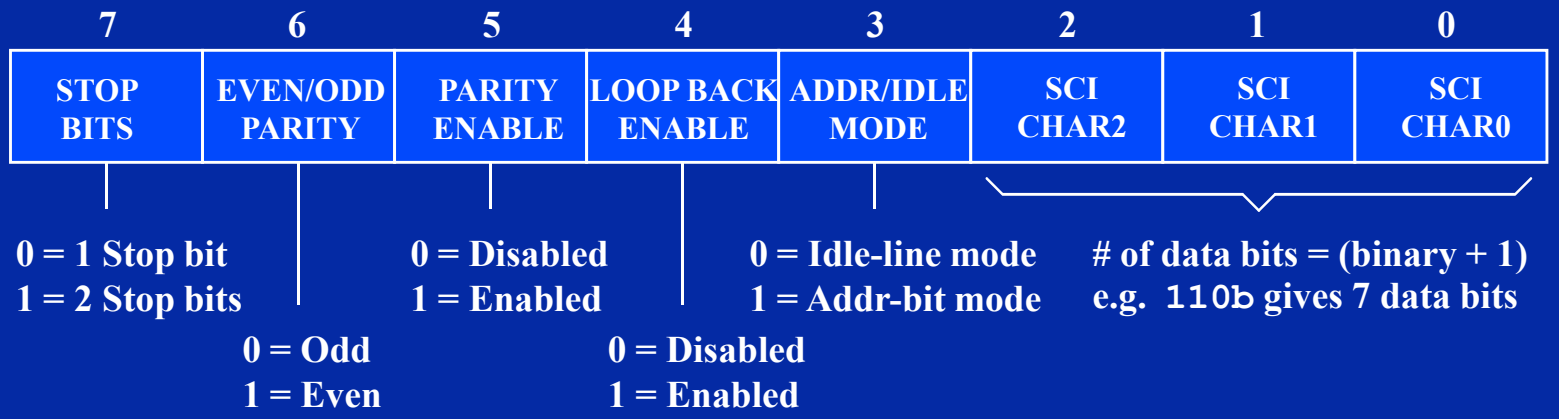
SCI – A Register Set

Address	Register	Name
0x007050	SCICCR	SCI-A communication control register
0x007051	SCICTL1	SCI-A control register 1
0x007052	SCIHBAUD	SCI-A baud register, high byte
0x007053	SCILBAUD	SCI-A baud register, low byte
0x007054	SCICTL2	SCI-A control register 2 register
0x007055	SCIRXST	SCI-A receive status register
0x007056	SCIRXEMU	SCI-A receive emulation data buffer
0x007057	SCIRXBUF	SCI-A receive data buffer register
0x007059	SCITXBUF	SCI-A transmit data buffer register
0x00705A	SCIFFTX	SCI-A FIFO transmit register
0x00705B	SCIFFRX	SCI-A FIFO receive register
0x00705C	SCIFFCT	SCI-A FIFO control register
0x00705F	SCIPRI	SCI-A priority control register

Note: Interface SCI – B Register Address space is 0x007750…0x00775F

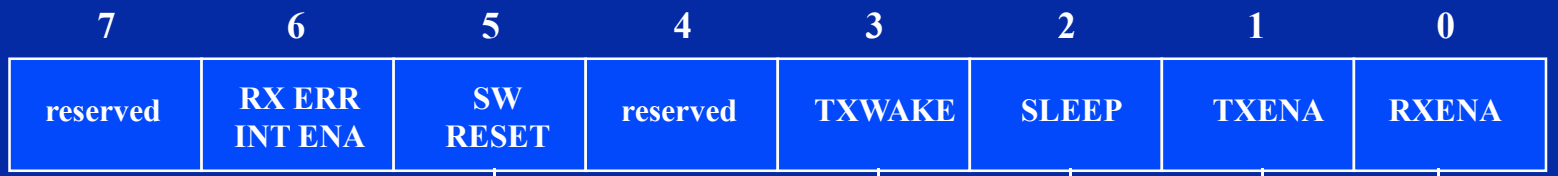
SCI-A Communication Control Register

Communications Control Register (SCICCR) – 0x007050



SCI-A Control Register 1

Control Register 1 (SCICTL1) – 0x007051



0 = receiver disabled
1 = receiver enabled

0 = transmitter disabled
1 = transmitter enabled

0 = sleep mode disabled
1 = sleep mode enabled

Transmitter wakeup method select
1 = wakeup mode depends on SCICCR.3
0 = no wakeup mode

Write 0 = Reset SCI
Write 1 = release from Reset

0 = Receive Error Interrupt disabled
1 = Receive Error Interrupt enabled

SCI-A Baud Rate

$$\text{SCI baud rate} = \begin{cases} \dfrac{\text{LSPCLK}}{(\text{BRR} + 1) \times 8}, & \text{BRR} = 1 \text{ to } 65535 \\ \dfrac{\text{LSPCLK}}{16}, & \text{BRR} = 0 \end{cases}$$

Baud-Select MSbyte Register (SCIHBAUD) – 0x007052

7	6	5	4	3	2	1	0
BAUD15 (MSB)	BAUD14	BAUD13	BAUD12	BAUD11	BAUD10	BAUD9	BAUD8

Baud-Select LSbyte Register (SCILBAUD) – 0x007053

7	6	5	4	3	2	1	0
BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0 (LSB)

SCI-A Control Register 2

SCICTL2 @ 0x007054

SCI RX/BK INT ENA

0 = Disable RXRDY/BRKDT interrupt
1 = Enable RXRDY/BRKDT interrupt

SCI TX EMPTY

0 = TXBUF or shift register are loaded with data
1 = Transmit buffer and shift register both empty

SCI TX READY

0 = SCITXBUF is full
1 = SCITXBUF is empty

SCI TX INT ENA

0 = Disable TXRDY interrupt
1 = Enable TXRDY interrupt

SCI-A Receiver Status Register

SCIRXST @ 0x007055

1 = Receiver wakeup condition detected

1 = Parity Error detected

1 = Overrun Error detected

1 = Framing Error detected

1 = Break condition occurred
0 = no break condition

0 = no new character in SCIRXBUF
1 = new character in SCIRXBUF

0 = No error flags set
1 = Error flag(s) set

SCI-A FIFO Transmit Register

SCIFFTX @ 0x00705A

SCI Reset
0 = reset
1 = enable operation

SCI FIFO Enhancements
0 = disable
1 = enable

TX FIFO Reset
0 = reset (pointer to 0)
1 = enable operation

TX FIFO Status (read-only)

00000	TX FIFO empty
00001	TX FIFO has 1 word
00010	TX FIFO has 2 words
00011	TX FIFO has 3 words
⋮	⋮
10000	TX FIFO has 16 words

15	14	13	12	11	10	9	8
SCIRST	SCIFFENA	TXFIFO RESET	TXFFST4	TXFFST3	TXFFST2	TXFFST1	TXFFST0

7	6	5	4	3	2	1	0
TXFFINT	TXFFINT CLR	TXFFIENA	TXFFIL4	TXFFIL3	TXFFIL2	TXFFIL1	TXFFIL0

TX FIFO Interrupt Flag (read-only)
0 = not occurred
1 = occurred

TX FIFO Interrupt Flag Clear
0 = no effect
1 = clear

TX FIFO Interrupt (on match) Enable
0 = disable
1 = enable

TX FIFO Interrupt Level
Interrupt when TXFFST4-0 and TXFFIL4-0 match

SCI-A FIFO Receive Register

SCIFFRX @ 0x00705B

RX FIFO Overflow Flag (read-only)
0 = no overflow
1 = overflow

RX FIFO Overflow Flag Clear
0 = no effect
1 = clear

RX FIFO Reset
0 = reset (pointer to 0)
1 = enable operation

RX FIFO Status (read-only)

00000	RX FIFO empty
00001	RX FIFO has 1 word
00010	RX FIFO has 2 words
00011	RX FIFO has 3 words
⋮	⋮
10000	RX FIFO has 16 words

15	14	13	12	11	10	9	8
RXFF-OVF	RXFF-OVF CLR	RXFIFO RESET	RXFFST4	RXFFST3	RXFFST2	RXFFST1	RXFFST0

7	6	5	4	3	2	1	0
RXFFINT	RXFFINT CLR	RXFFIEN	RXFFIL4	RXFFIL3	RXFFIL2	RXFFIL1	RXFFIL0

RX FIFO Interrupt Flag (read-only)
0 = not occurred
1 = occurred

RX FIFO Interrupt Flag Clear
0 = no effect
1 = clear

RX FIFO Interrupt (on match) Enable
0 = disable
1 = enable

RX FIFO Interrupt Level
Interrupt when RXFFST4-0 and RXFFIL4-0 match

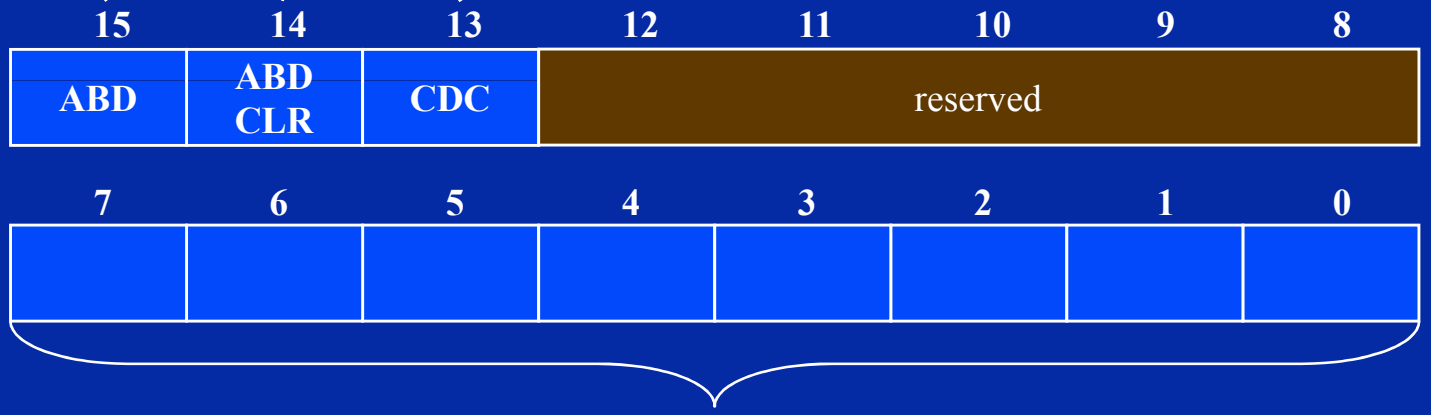
SCI-A FIFO Control Register

SCIFFCT @ 0x00705C

Auto Baud detection Flag (read-only)
0 = not complete
1 = complete

Auto Baud detection Flag Clear
0 = no effect
1 = clear

CDC calibrate 'A'
0 = disabled auto-baud alignment
1 = enables auto-baud alignment



FFTXDLY

Time delay between every transfer from FIFO to transmit shift register in number of SCI baud clock cycles (0 to 255)

Automatsko podašavanje brzine prenosa
Auto Baud

1. Enable auto baud-detect mode for the SCI by setting the CDC bit (bit 13) in SCIFFCT and clearing the ABD bit (Bit 15) by writing a 1 to ABDCLR bit (bit 14).
2. Initialize the baud register to be 1 or less than a baud rate limit of 500 Kbps.
3. Allow SCI to receive either character ‘A’ or ‘a’ from a host at the desired baud rate. If the first character is either 'A' or 'a', the auto baud- detect hardware will detect the incoming baud rate and set the ABD bit.
4. The auto-detect hardware will update the baud rate register with the equivalent baud value in hex. The logic will also generate an interrupt to the CPU.
5. Respond to the interrupt clear ADB bit by writing a 1 to ABD CLR (bit 14) of SCIFFCT register and disable further auto baud locking by clearing CDC bit by writing a 0.
6. Read the receive buffer for character ‘A’ or ‘a’ to empty the buffer and buffer status.
7. If ABD is set while CDC is 1, which indicates auto baud alignment, the SCI transmit FIFO interrupt will occur (TXINT). After the interrupt service CDC bit must be cleared by software.