Modul 8: Analogno Digitalni Konvertor

Digital Signal Controller
TMS320F2833x

Texas Instruments Incorporated

ADC Modul

- 12-bitna rezolucija
- Šesnaest ulaznih kanal sa naponskim opsegom 0…3V
- Relacija:

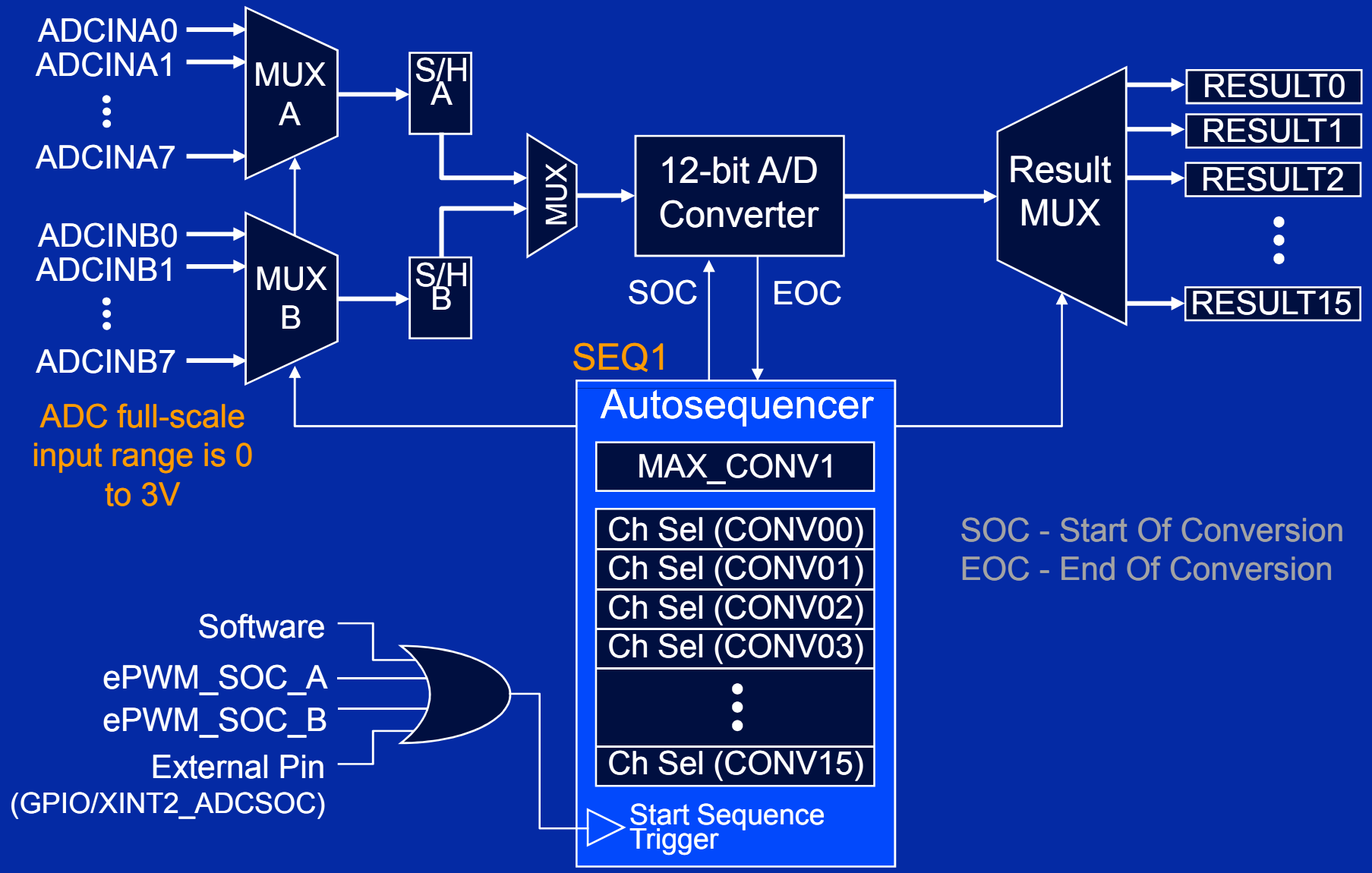
$$V_{in} = \frac{D * (V_{REF+} - V_{REF-})}{2^n - 1} + V_{REF-}$$

  - V_{in} = Analogni ulazni napon, opseg 0…3V
  - V_{ref+} = 3.0V V_{ref-} = 0V n = 12
  - D = digitalni rezultat, 12 Bitna rezolucija
- Maksimalna brzina konverzije: 12.5 MSPS (80 ns)
- Dva analogna ulazna multipleksera / dva SH kola
- Sekvencijalno i simultano odmeravanje
- Auto sekvenciranje – do 16 auto konverzija
- Šesnaest individualno adresabilnih registara za rezultat
- Izvori triger signala za *start-of-conversion*
  - External trigger, S/W or ePWM - Moduli

ADC režimi rada

- **Režim rada sekvencera:**
  - **Redni (Kaskadni – *Cascaded*) režim (16 stanja)**
  - **Dualni rad sekvencera (2 x 8 stanja)**
- **Režim odmeravanja:**
  - **Sekvencijalno odmeravanje (1 kanal u tenutku)**
  - **Simultano odmeravanje (2 kanala istovremeno)**
- **Režim startovanja:**
  - **Režim jedne sekvence (stop na kraju sekvence)**
  - **Kontinualni rad (*wrap* na kraju sekvence)**

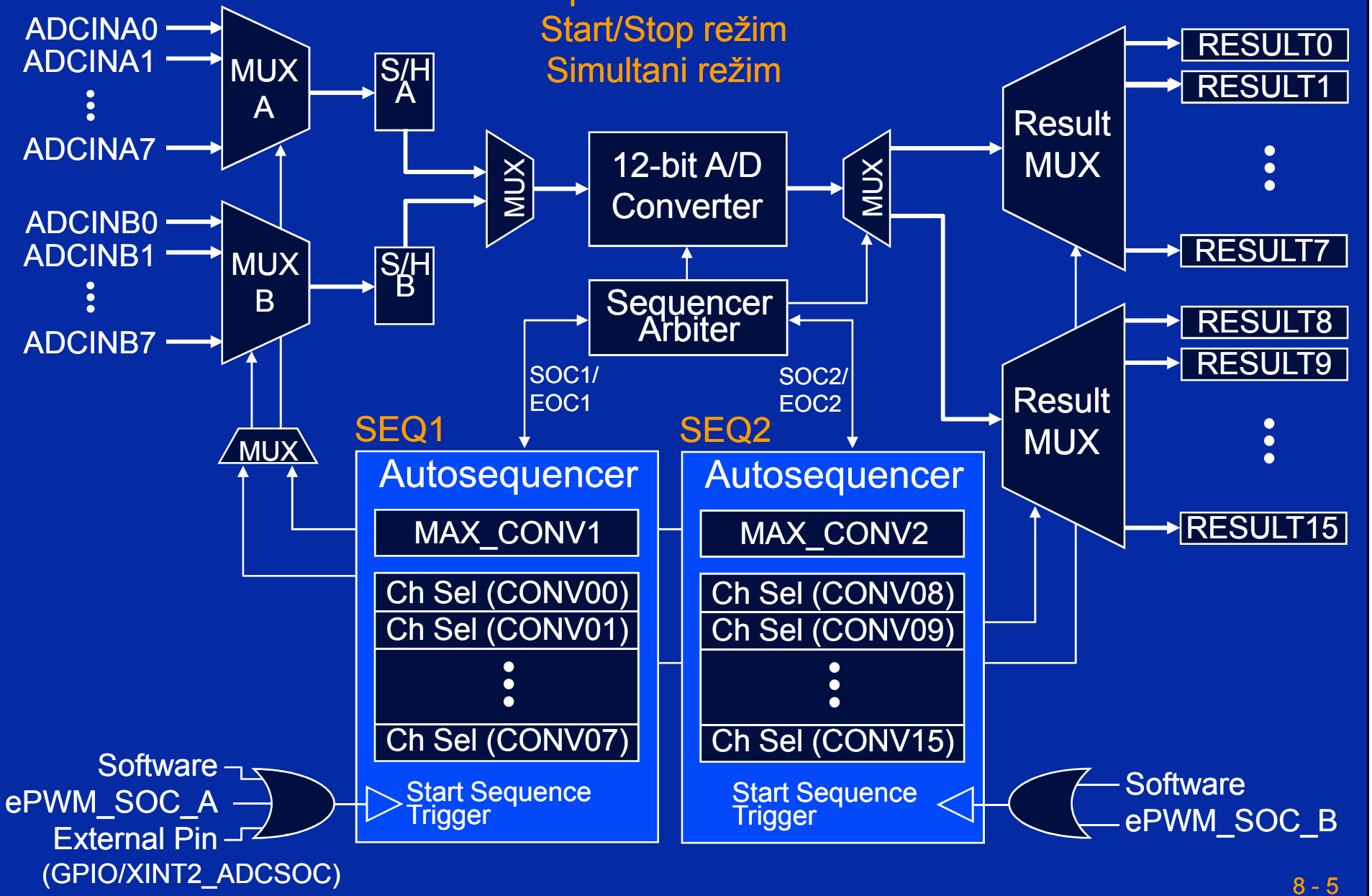
ADC Sekvencer *Cascaded* režimu



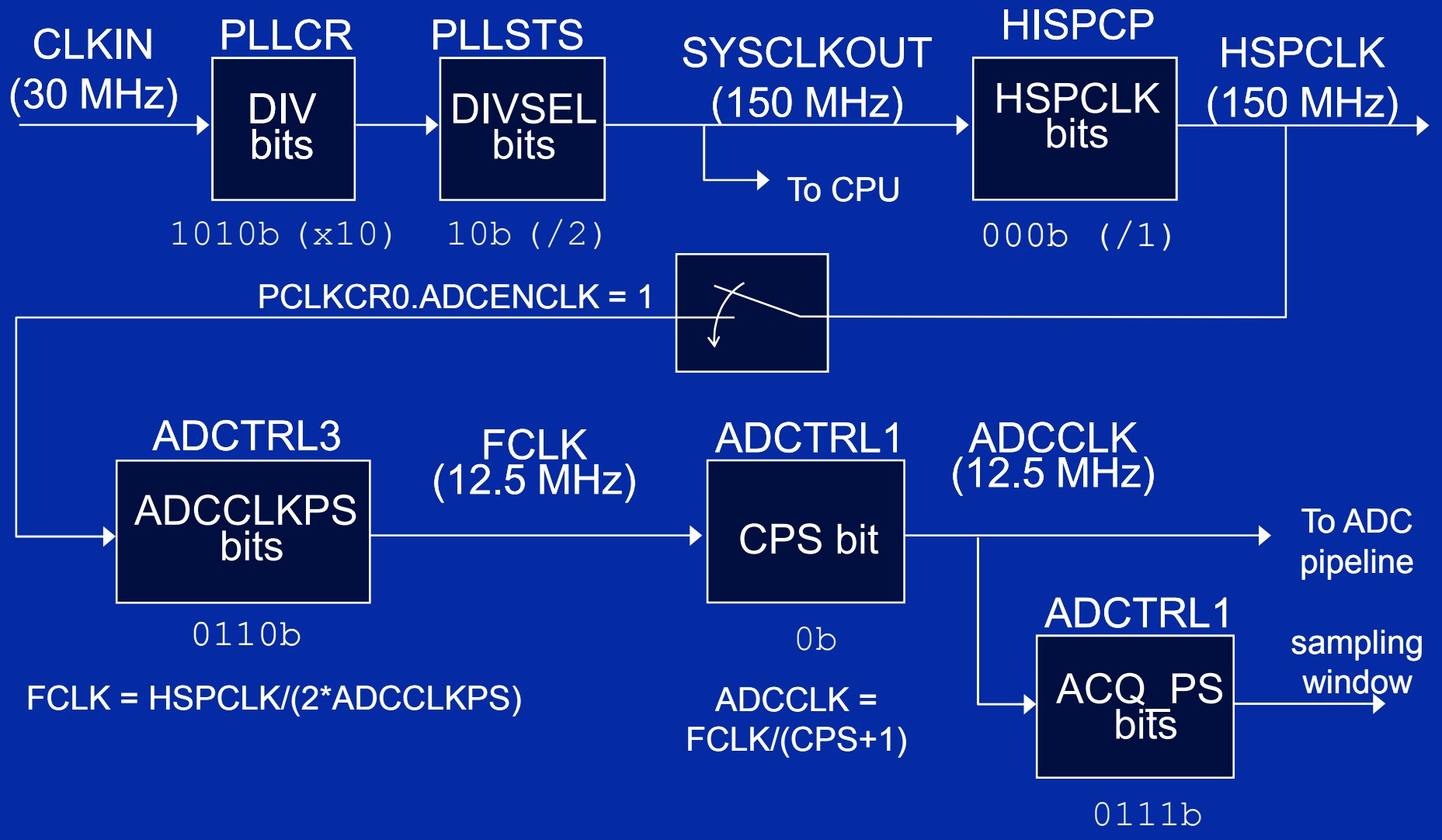
SOC - Start Of Conversion
EOC - End Of Conversion

ADC Sekvencer u dualnom radu

Neprekidani režim
Start/Stop režim
Simultani režim



Dijagram generisanja taktnog signala



Analog-to-Digital Converter Registers

Register	Description
ADCTRL1	ADC Control Register 1
ADCTRL2	ADC Control Register 2
ADCTRL3	ADC Control Register 3
ADCMAXCONV	ADC Maximum Conversion Channels Register
ADCCHSELSEQ1	ADC Channel Select Sequencing Control Register 1
ADCCHSELSEQ2	ADC Channel Select Sequencing Control Register 2
ADCCHSELSEQ3	ADC Channel Select Sequencing Control Register 3
ADCCHSELSEQ4	ADC Channel Select Sequencing Control Register 4
ADCASEQSR	ADC Autosequence Status Register
ADCRESULT0	ADC Conversion Result Buffer Register 0
ADCRESULT1	ADC Conversion Result Buffer Register 1
ADCRESULT2	ADC Conversion Result Buffer Register 2
⋮	⋮
ADCRESULT14	ADC Conversion Result Buffer Register 14
ADCRESULT15	ADC Conversion Result Buffer Register 15
ADCREFSEL	ADC Reference Select Register
ADCOFFTRIM	ADC Offset Trim Register
ADCST	ADC Status and Flag Register

ADC Control Register 1

Viši deo registra:

ADC Module Reset
0 = no effect
1 = reset (set back to 0 by ADC logic)

Acquisition Time Prescale (S/H)
ACQ Window = (ACQ_PS + 1)*(1/ADCCLK)

Emulation Suspend Mode
00 = free run (do not stop)
01 = stop after current sequence
10 = stop after current conversion
11 = stop immediately

Conversion Prescale
0: ADCCLK = FCLK / 1
1: ADCCLK = FCLK / 2

Struktura promenljive u C: AdcRegs.ADCTRL1

ADC Control Register 1

Niži deo registra:

Continuous Run
0 = stops after reaching end of sequence
1 = continuous (starts all over again from “initial state”)

Sequencer Mode
0 = dual mode
1 = cascaded mode

Sequencer Override
(functions only if CONT_RUN = 1)
0 = sequencer pointer resets to “initial state” at end of MAX_CONVn
1 = sequencer pointer resets to “initial state” after “end state” (7 ili 15)

Struktura promenljive u C : AdcRegs.ADCTRL1

ADC Control Register 2

Viši deo registra:

ePWM SOC B
(cascaded mode only)
0 = no action
1 = start by ePWM signal

Start Conversion (SEQ1)
0 = clear pending SOC trigger
1 = software trigger-start SEQ1

ePWM SOC A SEQ1 Mask Bit
0 = cannot be started by ePWM trigger
1 = can be started by ePWM trigger

Reset SEQ1
0 = no action
1 = immediate reset SEQ1 to “initial state”

Interrupt Enable (SEQ1)
0 = interrupt disable
1 = interrupt enable

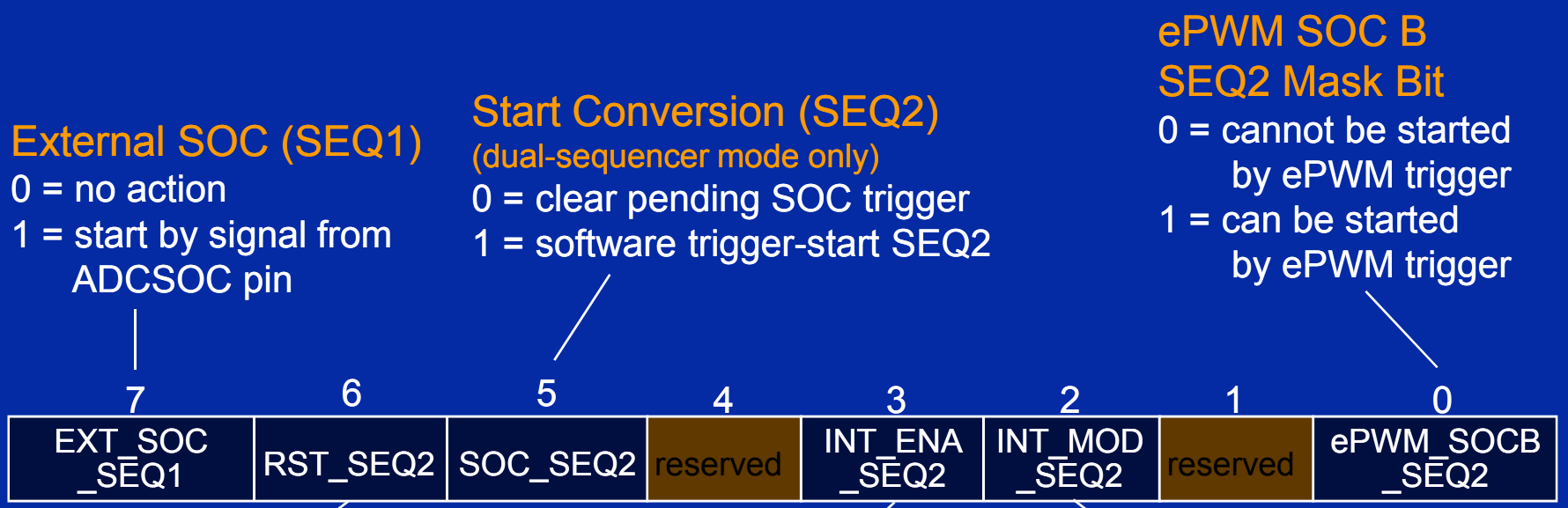
Interrupt Mode (SEQ1)
0 = interrupt every EOS
1 = interrupt every other EOS

Struktura promenljive u C: AdcRegs.ADCTRL2

EOS – End Of Sequence

ADC Control Register 2

Niži deo registra:



Struktura promenljive u C : AdcRegs.ADCTRL2

ADC Control Register 3

ADC Bandgap and Reference Power Down
00 = powered down
11 = powered up

ADC Power Down (except Bandgap & Ref.)
0 = powered down
1 = powered up

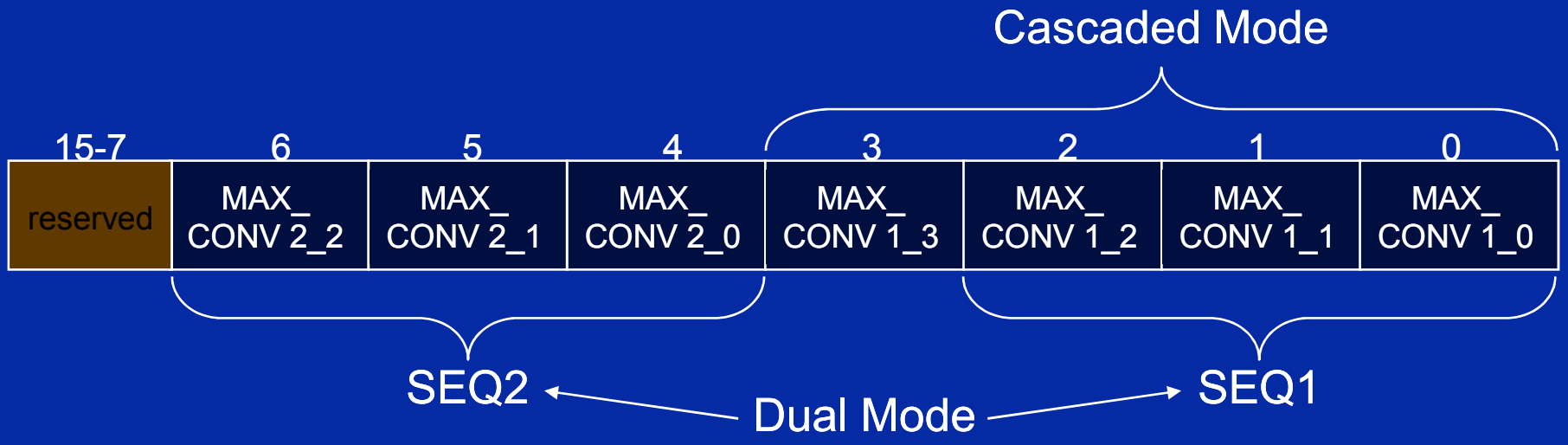
ADC Clock Prescale
0 : FCLK = HSPCLK
1 to F : FCLK = HSPCLK / (2*ADCCLKPS)

Sampling Mode Select
0 = sequential sampling mode
1 = simultaneous sampling mode

Struktura promenljive u C : AdcRegs.ADCTRL3

Registar za broj maksimalnih konverzija

- Bitska polja definišu broj konverzija po jednom triger signalu (binary+1)



- Svaki sekvencer počinenje sa “Initial state” i uvećava ga sekvencijalno
- Svaki *wrap*-uje sa “end state” ako ga pre toga nije softver resetovao

	SEQ1	SEQ2	Cascaded
Initial state	CONV00	CONV08	CONV00
End state	CONV07	CONV15	CONV15

Struktura promenljive u C : AdcRegs.ADCMAXCONV

Regostar za selekciju ulaznih kanala

	15 - 12	11 - 8	7 - 4	3 - 0
ADCCHSELSEQ1	CONV03	CONV02	CONV01	CONV00
ADCCHSELSEQ2	CONV07	CONV06	CONV05	CONV04
ADCCHSELSEQ3	CONV11	CONV10	CONV09	CONV08
ADCCHSELSEQ4	CONV15	CONV14	CONV13	CONV12

Ulazni kanali ADC broje se binarno:

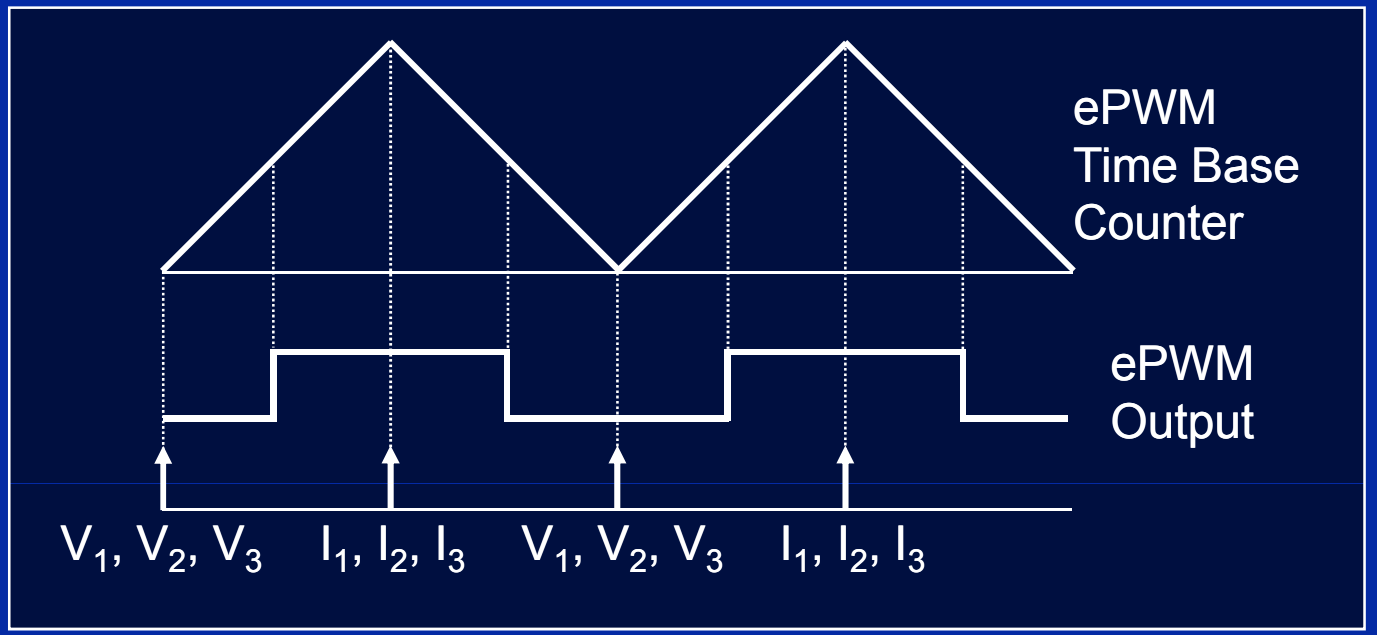
ADCINA0 = 0000 ADCINB0 = 1000

ADCINA1 = 0001 ….

… ADCINB7 = 1111

Struktura promenljive u C : AdcRegs.ADCCHSELSEQ1 … AdcRegs.ADCCHSELSEQ4

Primer – Sekvencer u “Start/Stop” režimu



Konfiguracioni zahtevi:

- **ePWM triggerruje ADC**
  - **Tri auto konverzije (V1, V2, V3) za *trigger 1* (CTR = 0)**
  - **Tri auto konverzije (I1, I2, I3) za *trigger 2* (CTR = PRD)**
- **Sekvencer u kaskadnom režimu a odmeravanje u sekvencijalnom režimu**

Primer – Sekvencer u “Start/Stop” režimu

- **MAX_CONV1 postavljen na 2 a registar za selekciju ulaznih kanala na:**

Bits →	15-12	11-8	7-4	3-0	
	I_1	V_3	V_2	V_1	ADCCHSELSEQ1
	x	x	I_3	I_2	ADCCHSELSEQ2

- **Nakon reseta i inicijalizacije, SEQ1 čeka na triger**
- **Na prvi triger izvršavaju se tri konverzije: CONV00 (V1), CONV01 (V2), CONV02 (V3)**
- **SEQ1 čeka na drugi triger**
- **Na drugi triger izvršavaju se konverzije: CONV03 (I1), CONV04 (I2), CONV05 (I3)**
- **Na kraju druge sekvence, registri za rezultat imaju sledeće vrednosti:**

RESULT0	V_1
RESULT1	V_2
RESULT2	V_3
RESULT3	I_1
RESULT4	I_2
RESULT5	I_3

- **SEQ1 čeka u tekućem stanju na drugi triger**
- **ISR čita rezultat i resetuje SEQ1**

Registri za rezultat konverzije

AdcRegs.ADCRESULTx, x = 0 - 15 (2 wait-state read)

AdcMirror.ADCRESULTx, x = 0 - 15 (0 wait-state read)

Input Voltage	Digital Result	AdcRegs. ADCRESULTx	AdcMirror. ADCRESULTx
3.0	0xFFF	1111|1111|1111|0000	0000|1111|1111|1111
1.5	0x7FF	0111|1111|1111|0000	0000|0111|1111|1111
0.00073	1	0000|0000|0001|0000	0000|0000|0000|0001
0	0	0000|0000|0000|0000	0000|0000|0000|0000

Odmeravanje bipolarnih signal

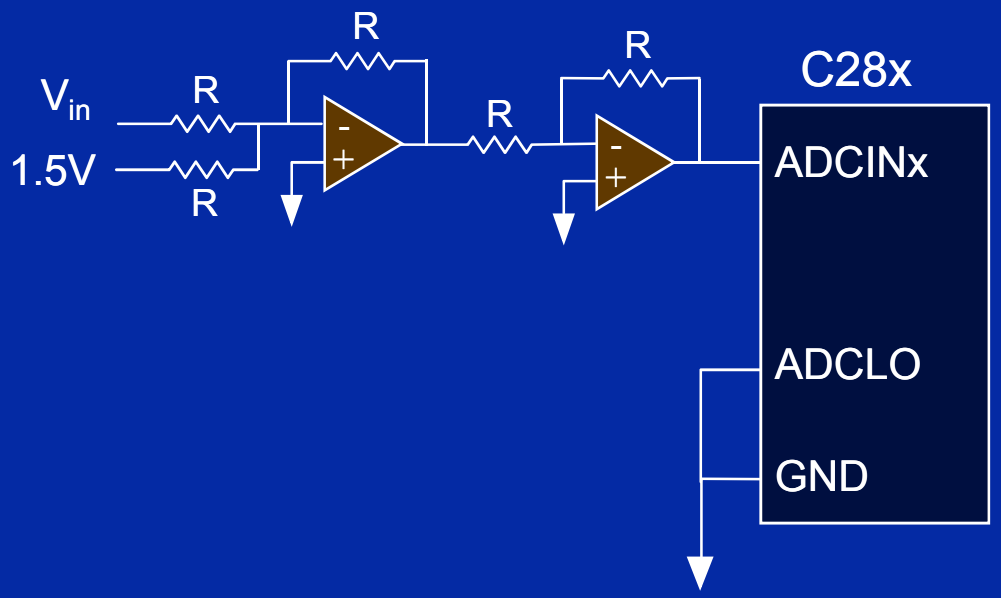
Primer: $-1.5\ V \leq V_{in} \leq +1.5\ V$

1) Dodavanje 1.5 volti
   analognom ulazu

Odmeravanje bipolarnih signal

Primer: -1.5 V ≤ V_{in} ≤ +1.5 V

1) Dodavanje 1.5 volti analognom ulazu



Odmeravanje bipolarnih signal

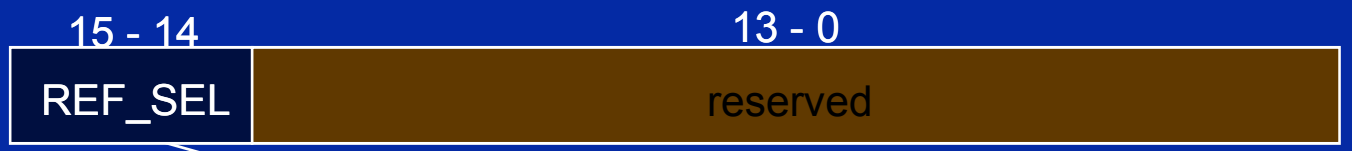
2) Subtract “1.5” from the digital result

```
#include “DSP2833x_Device.h”
#define  offset  0x07FF
void main(void)
{
   int16 value;              // signed

   value = AdcMirror.ADCRESULT0 – offset;
}
```

Izbor referentnog signala ADC

- ADC F28335 poseduje ugrađeni referentni signal sa temperaturnom stabilnosti ~50 PPM/°C *
- Mogućnost korišćenja spoljašnje reference
  - Izbor spoljašnje reference: 2.048 V, 1.5 V, 1.024 V
  - Referenca NE MENJA ulazni opseg pune skale 0 - 3 V
- Registar za izbor referentnog signala ADCREFSEL



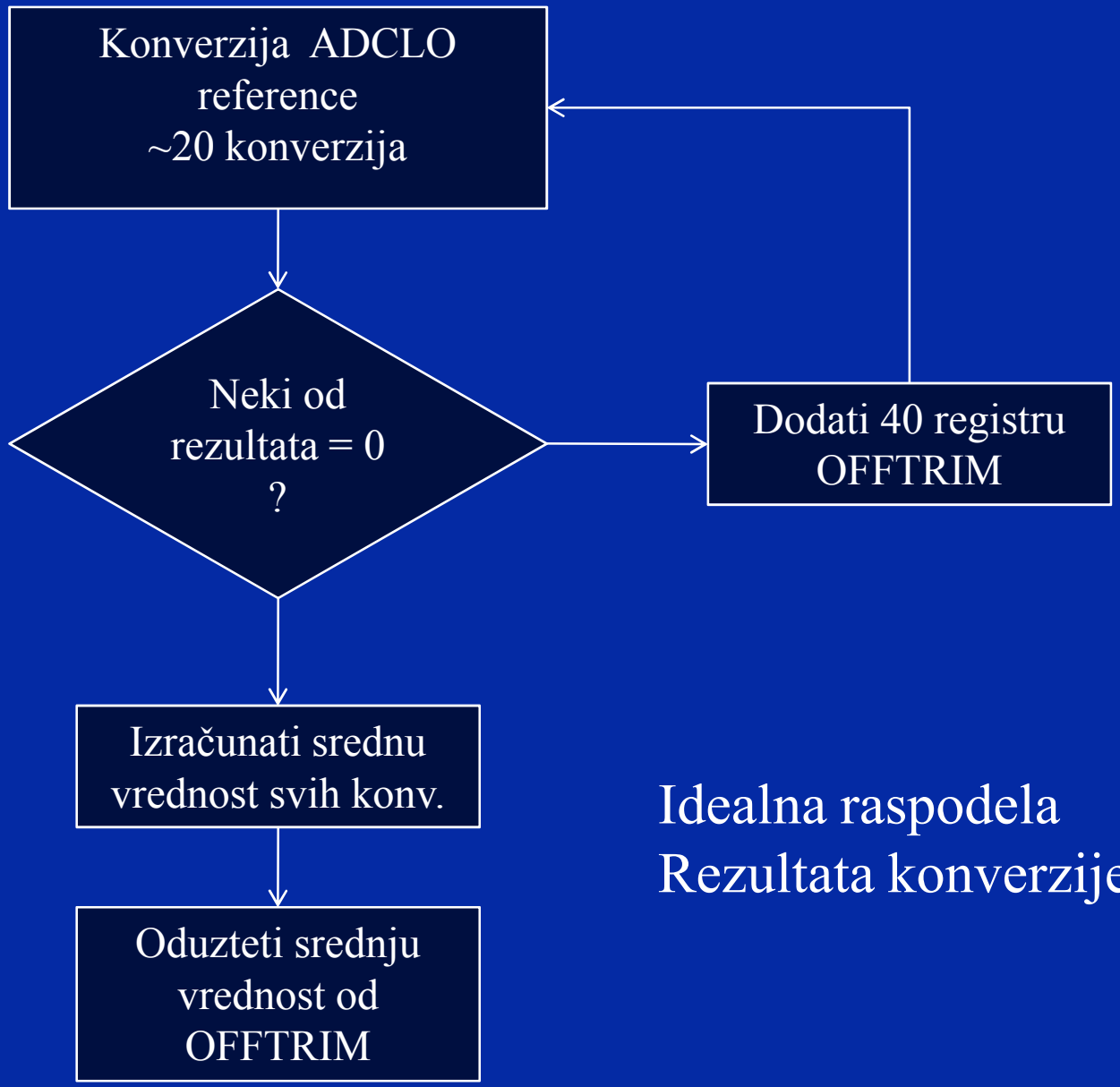
ADC Reference Selection
00 = internal (default)
01 = external 2.048 V
10 = external 1.5 V
11 = external 1.024 V

Struktura promenljive u C : AdcRegs.ADCREFSEL

Korekcija ofseta

- Registar ADCOFFTRIM (9-bitno polje -256/255)
  Vrednost sa kojem se rezultat konverzije sabira/oduzima pre smeštanja u registre za rezultat
- Tajming nije poremećen
- Održanje punog dinamičkog opsega
- Sadržaj ADCOFFTRIM registra definiše se u ADC_cal rutini boot ROM-a

Korekcija ofseta



Idealna raspodela Rezultata konverzije