

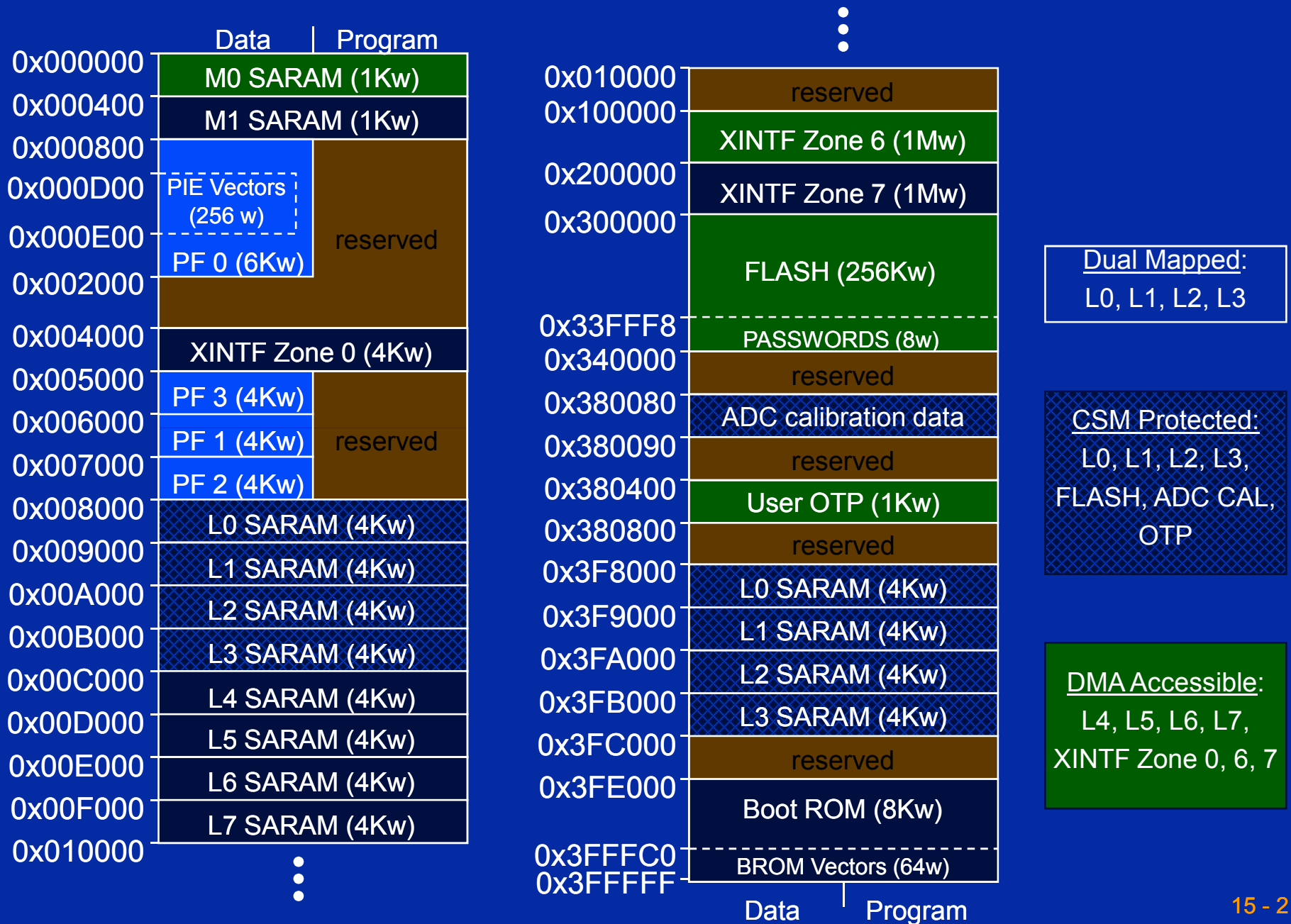
# Modul 15: Boot-ROM i Boot-Loader

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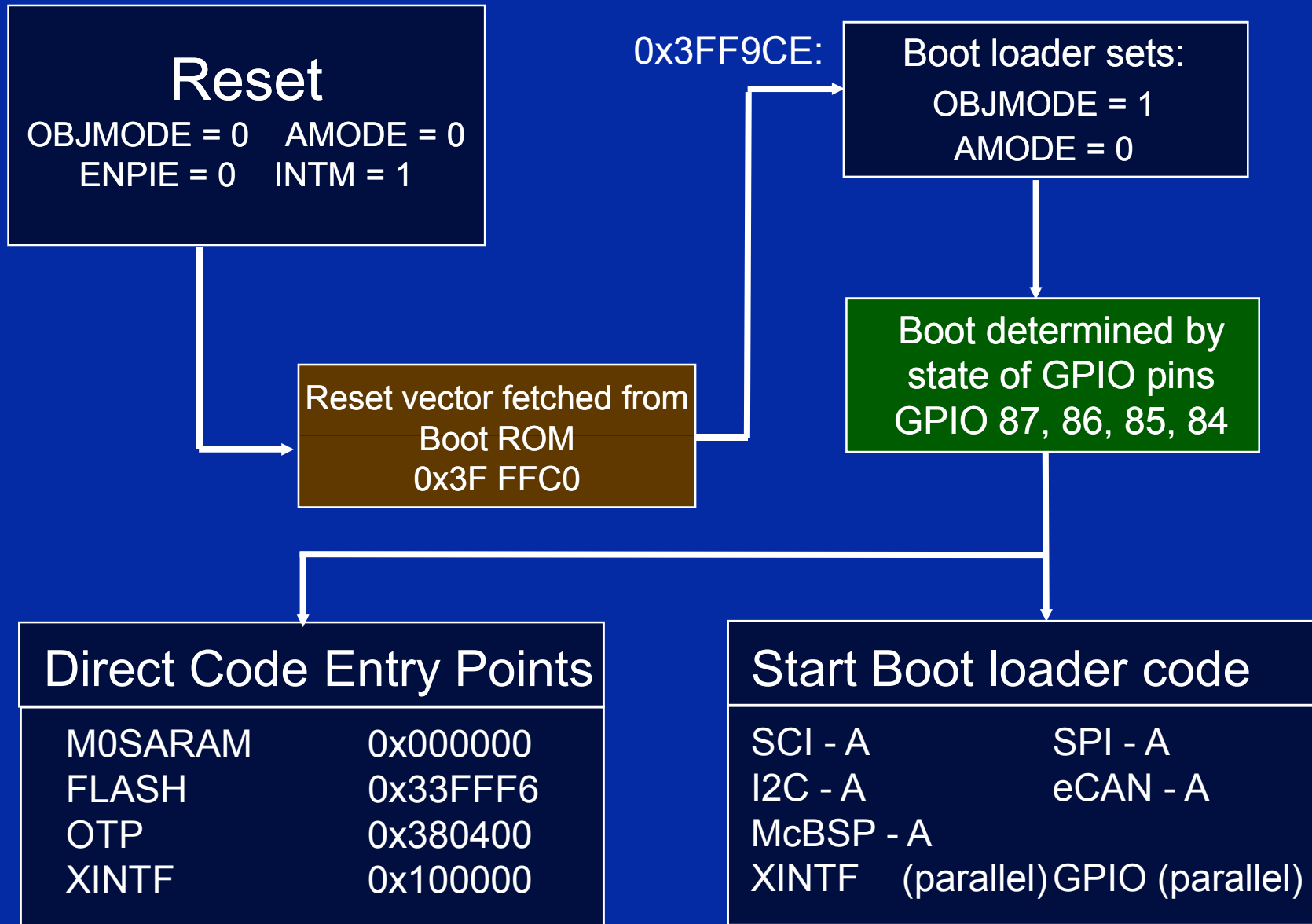
**32-Bit-Digital Signal Controller  
TMS320F2833x**

**Texas Instruments Incorporated**

# TMS320F2833x Memory Map



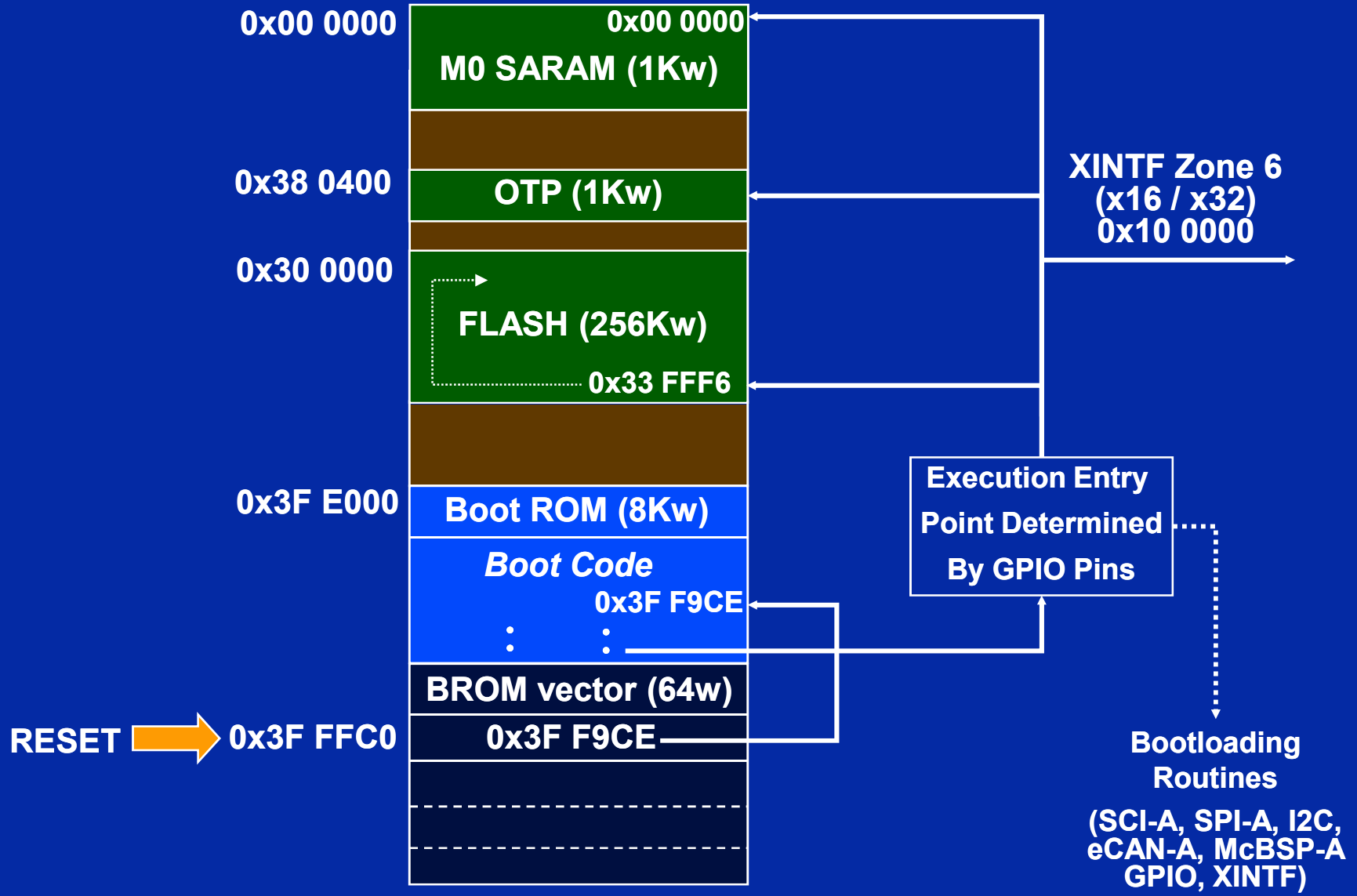
# Reset – Bootloader



# Boot Loader Options

GPIO pins				Boot Mode	
87	86	85	84		
1	1	1	1	jump to <b>FLASH</b>	address 0x33 FFF6
0	1	0	0	jump to <b>M0 SARAM</b>	address 0x00 0000
0	1	1	1	jump to <b>OTP</b>	address 0x38 0400
1	0	0	1	jump to <b>XINTF 16</b>	address 0x10 0000
1	0	0	0	jump to <b>XINTF 32</b>	address 0x10 0000
1	1	1	0	boot load code to on-chip memory via <b>SCI - A</b> port	
1	1	0	1	boot load code to on-chip memory via <b>SPI - A</b> port	
1	1	0	0	boot load code to on-chip memory via <b>I2C - A</b> port	
1	0	1	1	boot load code to on-chip memory via <b>eCAN - A</b> port	
1	0	1	0	boot load code to on-chip memory via <b>McBSP - A</b> port	
0	1	1	0	boot load code to on-chip memory via <b>GPIO</b> (parallel)	
0	1	0	1	boot load code to on-chip memory via <b>XINTF</b> (parallel)	

# Reset Code Flow - Summary



# F2833x BOOT-ROM Memorijaska mapa

Address Range	Function	Format
0x3FE000 – 0x3FE501	IQ - Math sine/cosine table	641 x 32 bit; I2Q30
0x3FE502 – 0x3FE711	IQ - Math normalized inverse	264 x 32 bit; I3Q29
0x3FE712 – 0x3FE823	IQ - Math normalized sqrt	137 x 32 bit; I2Q30
0x3FE824 – 0x3FE9E7	IQ - Math normalized arctan	226 x 32 bit; I2Q30
0x3FE9E8 – 0x3FEB4F	IQ – Math round / saturation	180 x 32 bit; I2Q30
0x3FEB50 – 0x3FEBBC7	IQ – Math min / max table	60 x 32 bit; I31Q1 – I1Q31
0x3FEBBC8 – 0x3FEBDB	IQ – Math exp(x) table	10 x 32 bit; I1Q31
0x3FEBDC – 0x3FF0DD	FPU sine/cosine table	641 x 32 bit; float
0x3FF0DE – 0x3FF261	FPU normalized arctan	194 x 32 bit; float
0x3FF262 – 0x3FF275	FPU exp(x) table	10 x 32 bit; float
0x3FF276 – 0x3FF34B	reserved	
0x3FF34C – 0x3FF9ED	Boot Loader Functions	F2833x machine code
0x3FF9EE – 0x3FFFB8	reserved	
0x3FFFB9 – 0x3FFFBF	ROM version and	
0x3FFFC0 – 0x3FFFFFF	Reset and Interrupt vectors	32 x 32 bit address

# F2833x BOOT-ROM vektor tabela

Vector	Address	Content
<b>RESET</b>	0x3F FFC0	0x3F FC00
<b>INT1</b>	0x3F FFC2	0x00 0042
<b>INT2</b>	0x3F FFC4	0x00 0044
<b>INT3</b>	0x3F FFC6	0x00 0046
<b>INT4</b>	0x3F FFC8	0x00 0048
<b>INT5</b>	0x3F FFCA	0x00 004A
<b>INT6</b>	0x3F FFCC	0x00 004C
<b>INT7</b>	0x3F FFCE	0x00 004E
<b>INT8</b>	0x3F FFD0	0x00 0050
<b>INT9</b>	0x3F FFD2	0x00 0052
<b>INT10</b>	0x3F FFD4	0x00 0054
<b>INT11</b>	0x3F FFD6	0x00 0056
<b>INT12</b>	0x3F FFD8	0x00 0058
<b>INT13</b>	0x3F FFDA	0x00 005A
<b>INT14</b>	0x3F FFDC	0x00 005C
<b>DLOGINT</b>	0x3F FFDE	0x00 005E

Vector	Address	Content
<b>RTOSINT</b>	0x3F FFE0	0x00 0060
<b>reserved</b>	0x3F FFE2	0x00 0062
<b>NMI</b>	0x3F FFE4	0x00 0064
<b>ILLEGAL</b>	0x3F FFE6	0x00 0066
<b>USER 1</b>	0x3F FFE8	0x00 0068
<b>USER 2</b>	0x3F FFEA	0x00 006A
<b>USER 3</b>	0x3F FFEC	0x00 006C
<b>USER 4</b>	0x3F FFEE	0x00 006E
<b>USER 5</b>	0x3F FFF0	0x00 0070
<b>USER 6</b>	0x3F FFF2	0x00 0072
<b>USER 7</b>	0x3F FFF4	0x00 0074
<b>USER 8</b>	0x3F FFF6	0x00 0076
<b>USER 9</b>	0x3F FFF8	0x00 0078
<b>USER 10</b>	0x3F FFFA	0x00 007A
<b>USER 11</b>	0x3F FFFC	0x00 007C
<b>USER 12</b>	0x3F FFFE	0x00 007E

# Boot Loader: Struktura niza podataka

1	0x10AA : Key for memory width = 16 bit
2-9	Reserved for future use
10	Entry Point PC[22:16]
11	Entry Point PC[15:0]
12	Block Size (words); if 0 then end of transmission
13	Destination Address of block ; Addr[31:16]
14	Destination Address of block ; Addr[15:0]
15	First word of block

○

N	Last word of block
N+1	Block Size (words)
N+2	Destination Address of block ; Addr[31:16]
N+3	Destination Address of block ; Addr[15:0]

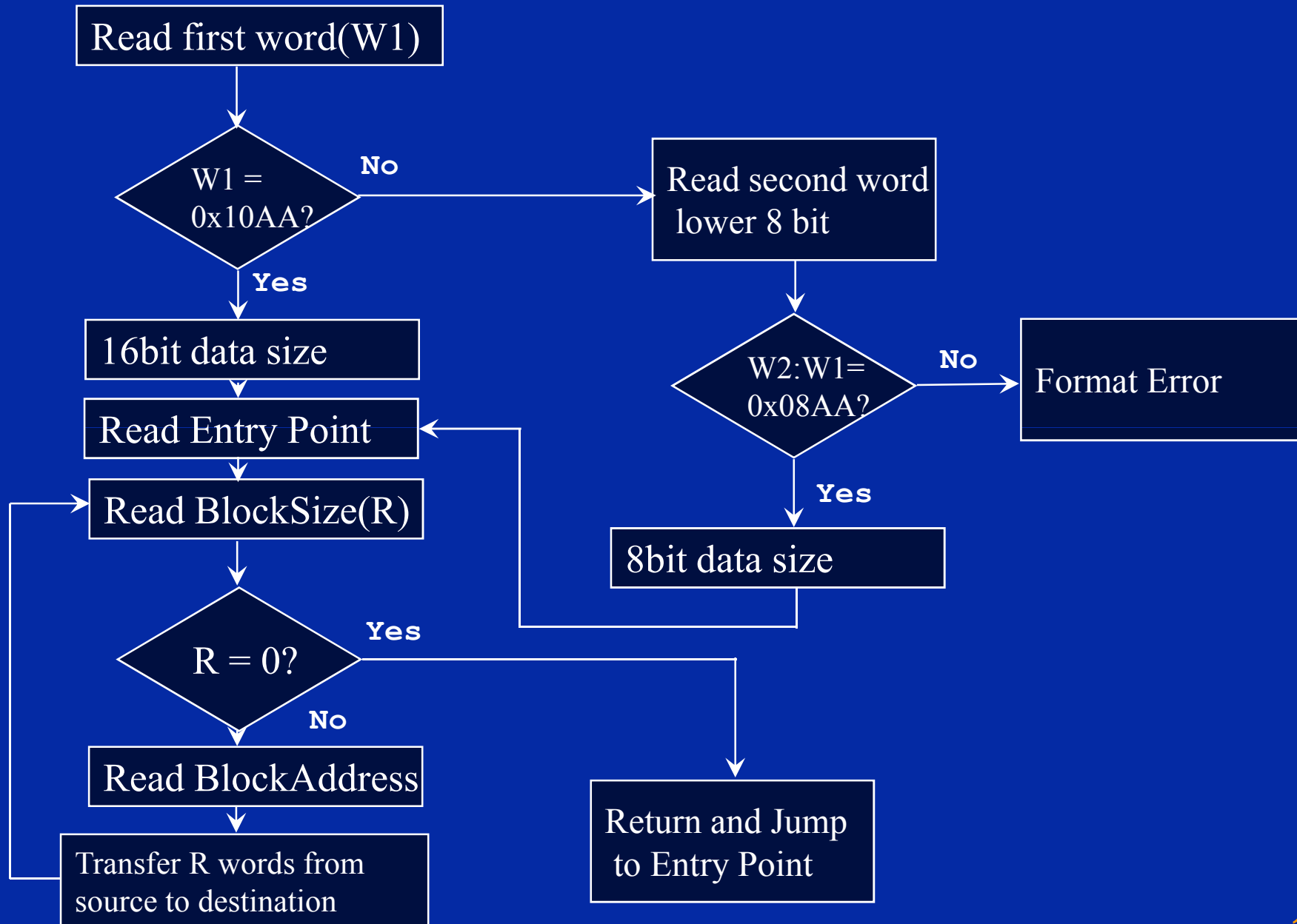
○



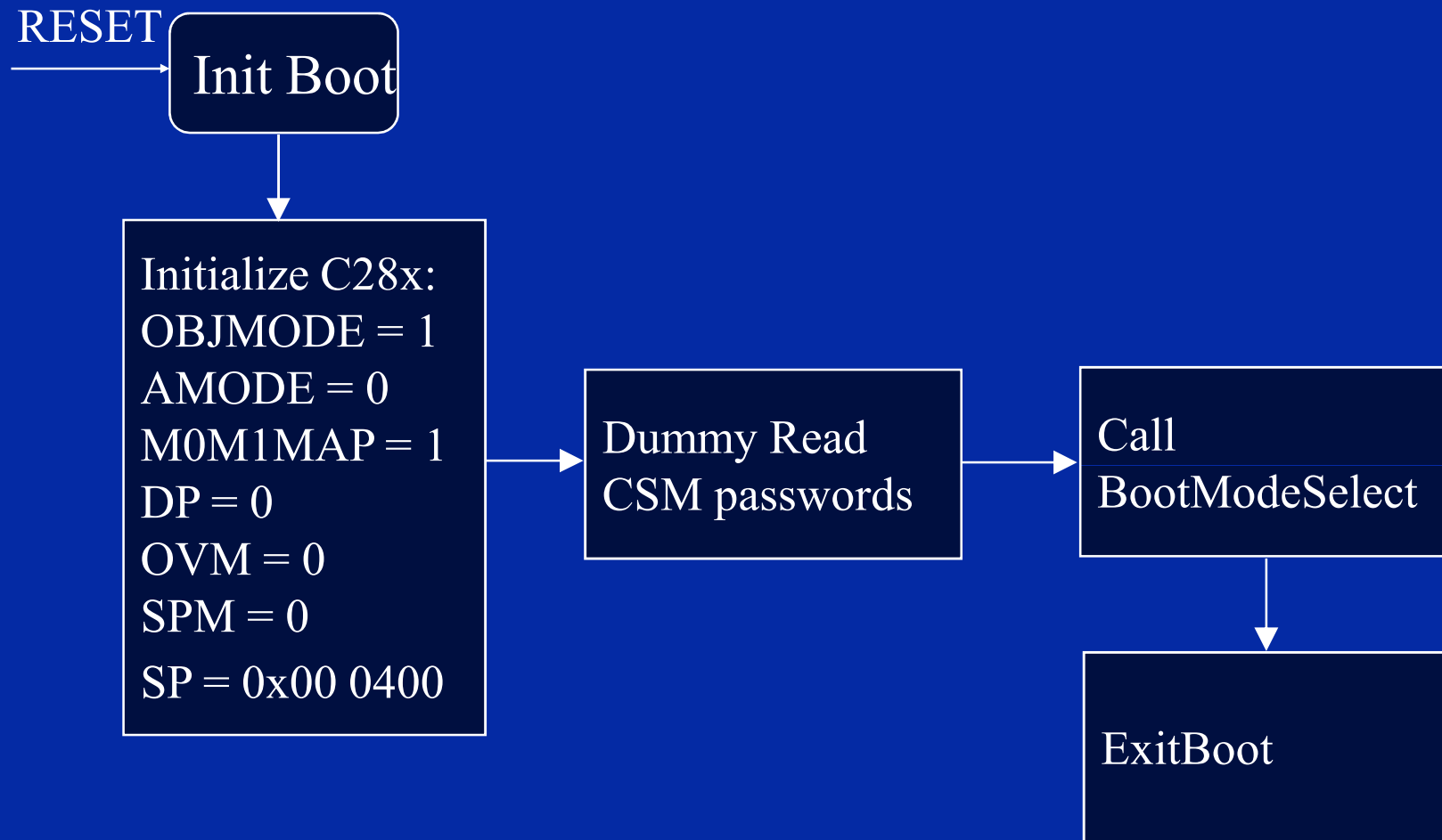
# Boot Loader Data Stream Example

```
10AA      ; Key for 16-Bit memory stream
0000
0000
0000
0000
0000
0000
0000
0000
0000
0000
003F      ; PC - starting point after load is complete: 0x3F 8000
8000
0005      ; 5 words in block 1
003F
9010      ; First block is loaded into 0x3F 9010
0001      ; first data word
0002
0003
0004
0005      ; last data
0002      ; Second block is two words long
003F      ; Second block is loaded into 0x3F 8000
8000
7700      ; first data
7625      ; last data
0000      ; next block zero length = end of transmission
```

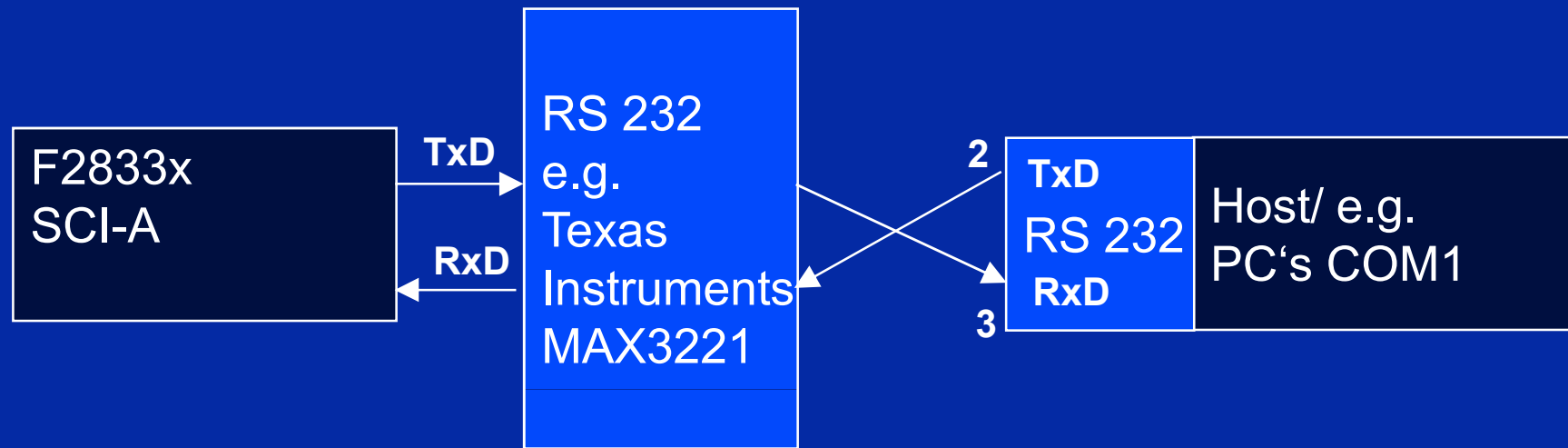
# Procedura transfera podataka



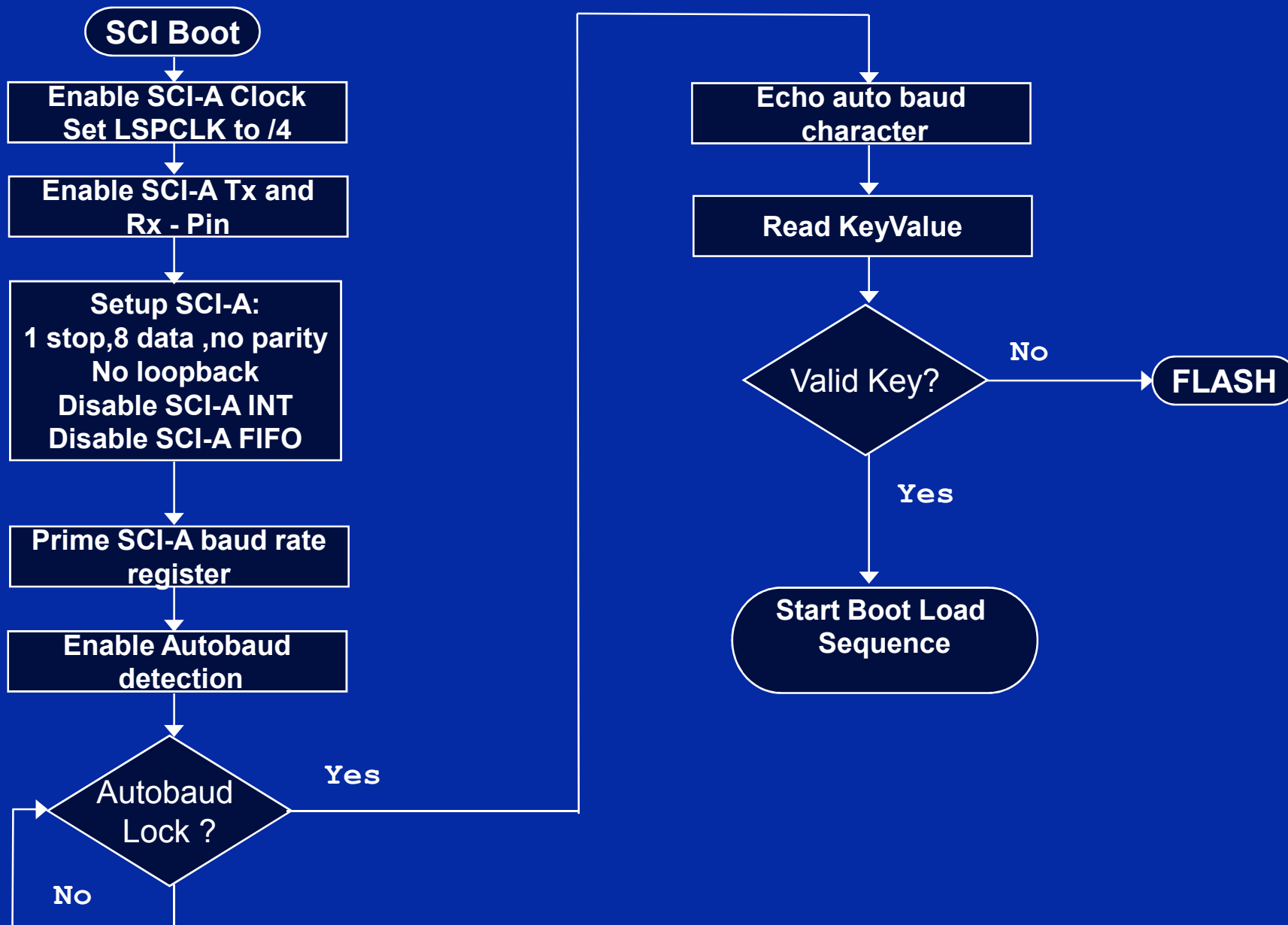
# F2833x Init Boot Function



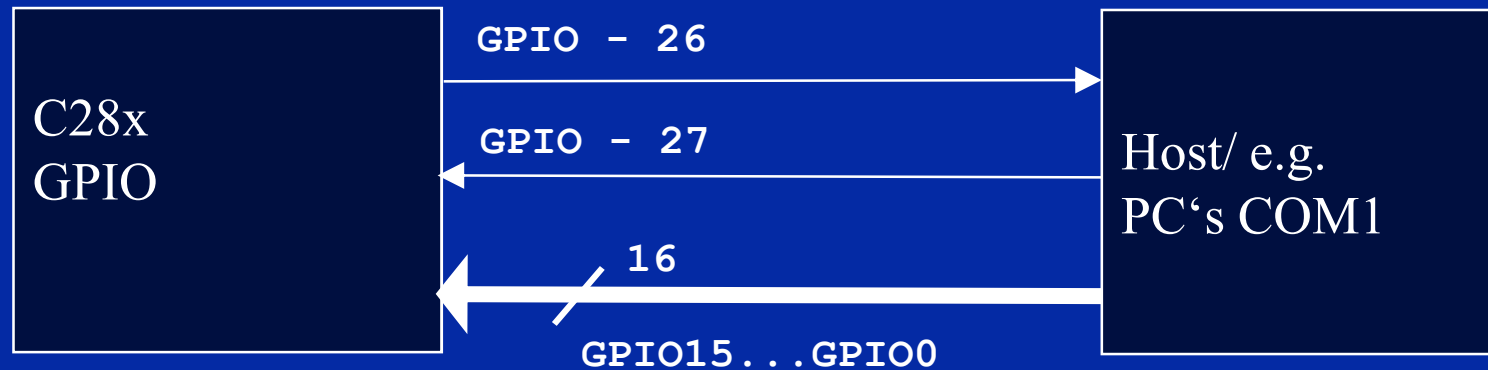
# F2833x SCI Boot Loader Function



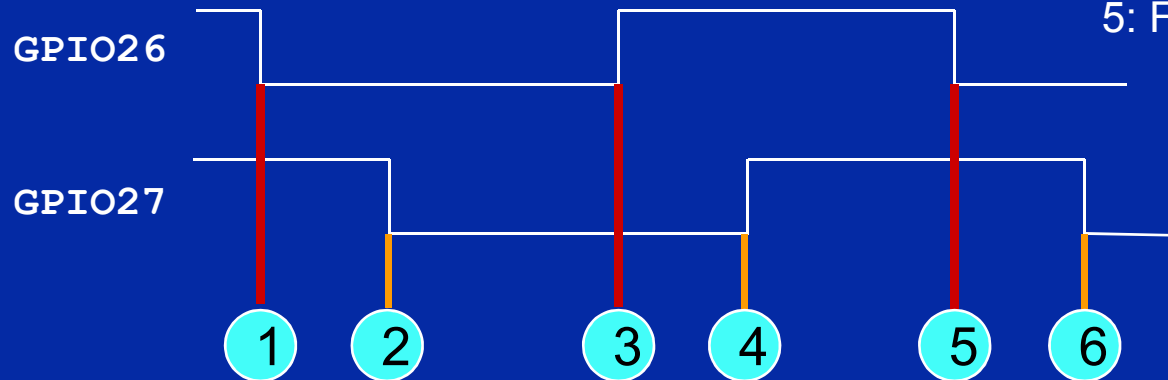
# F2833x SCI Boot Function



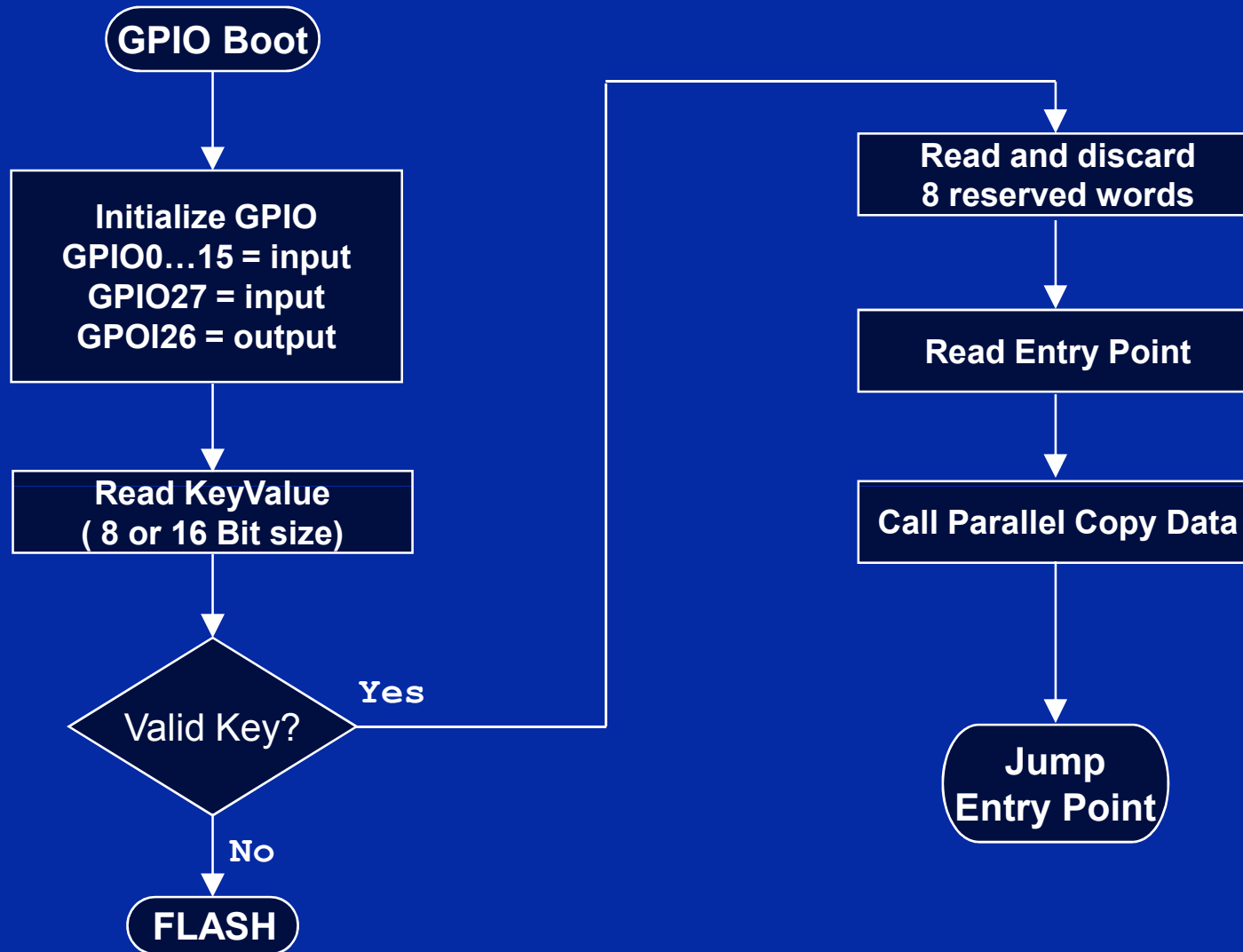
# F2833x parallel Boot Loader (GPIO)



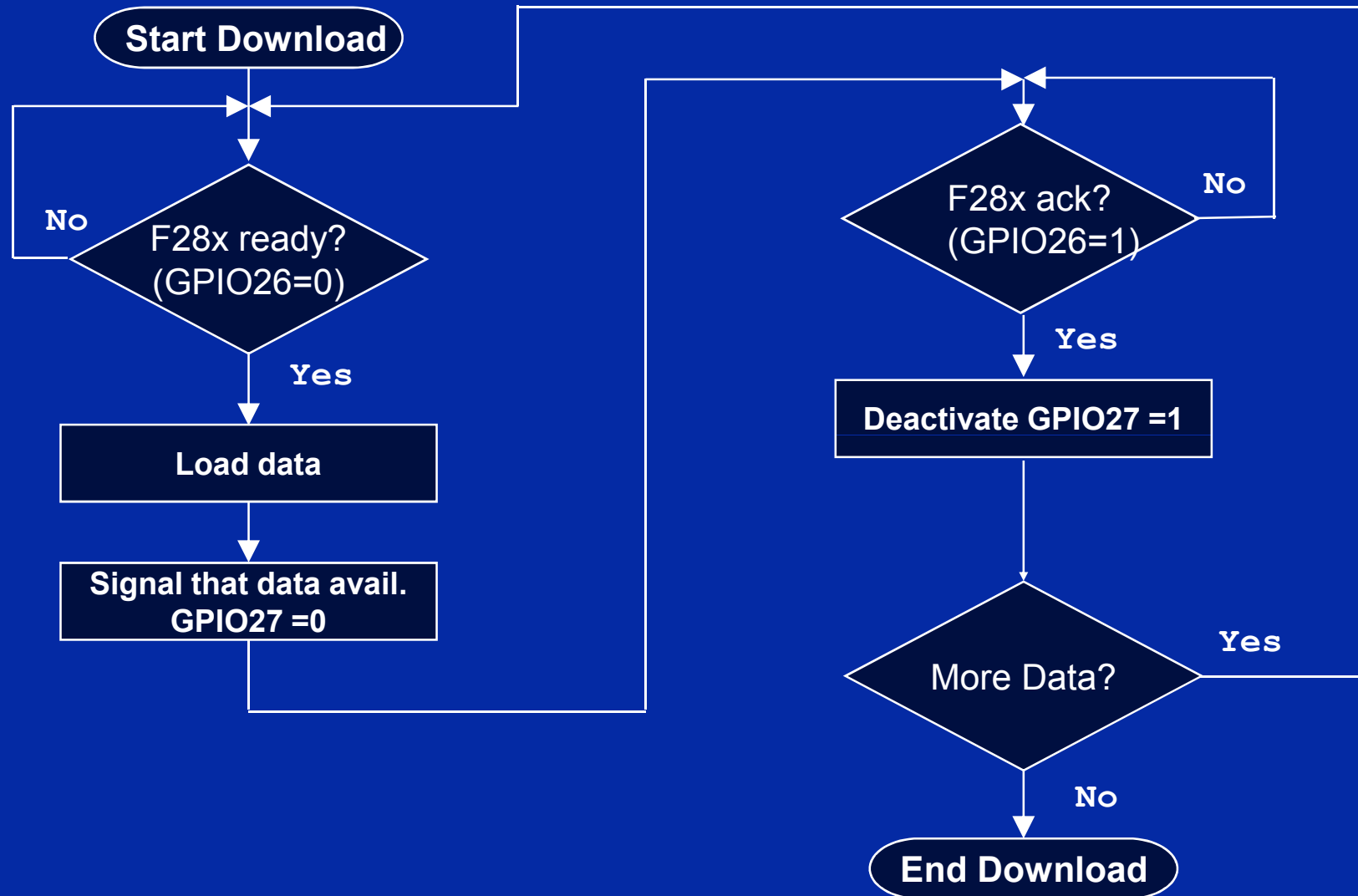
- 1: F28x indicates: "ready to receive"
- 2: Host signals "data active at GPIO-B"
- 3: F28x indicates "read is complete"
- 4: Host acknowledges "cycle completed"
- 5: F28x indicates: "ready for more data"



# F2833x GPIO Boot Function

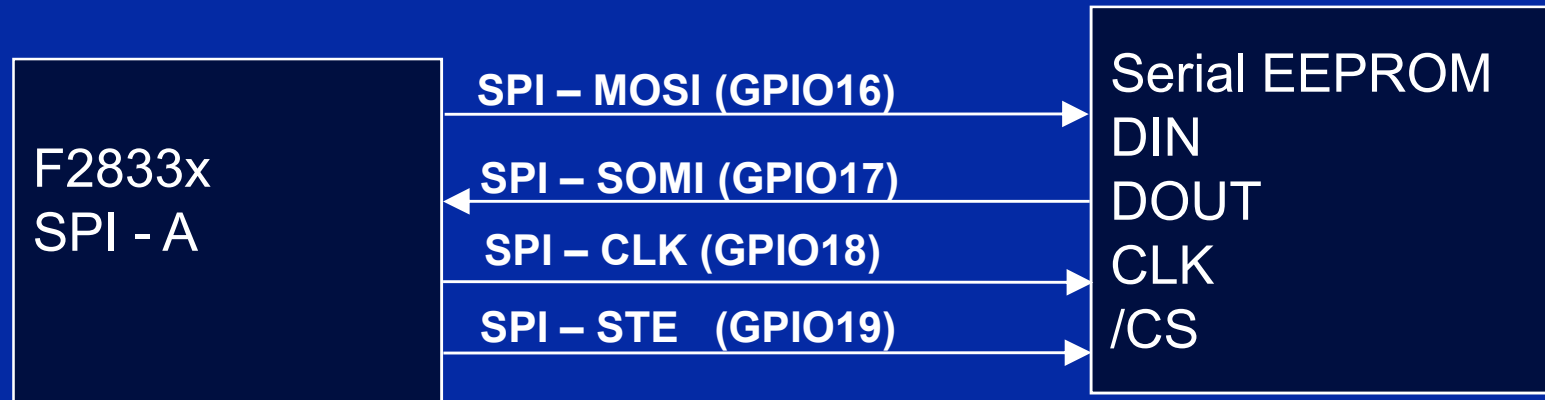


# Host GPIO Boot Function





# F2833x SPI Boot Loader Function



## Note:

- (1) SPI – loader is 8bit only, it does not support 16bit data stream
- (2) EEPROM data stream must start at address 0x0000

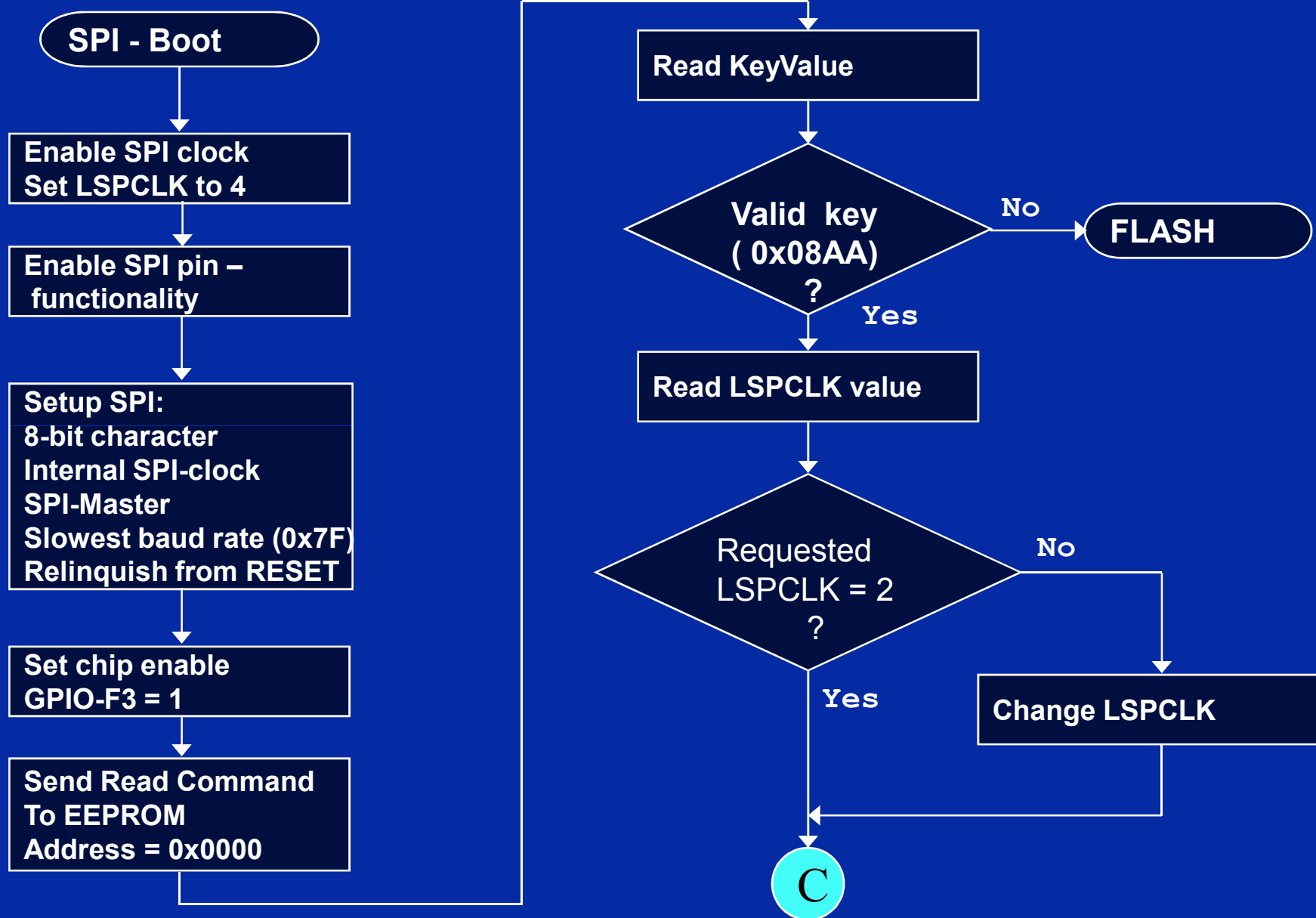
## EEPROM – Types:

Atmel: AT25C256; see chapter 13  
Xicor: X25256  
ST: M95080  
and others

# F2833x SPI Boot Loader Data Stream

Byte	Content
1	LSB = 0xAA ( Key for 8bit transfer)
2	MSB = 0x08 ( Key for 8bit transfer)
3	LSB = LSPCLK value
4	MSB = SPIBRR value
5-18	reserved
19	Entry Point [23:16]
20	Entry Point [31:24]
21	Entry Point [7:0]
22	Entry Point [15:8]
23 ...	Blocks of data: block size/destination/data as shown

# F2833x SPI Boot Function



# F2833x SPI Boot Function (cont.)

