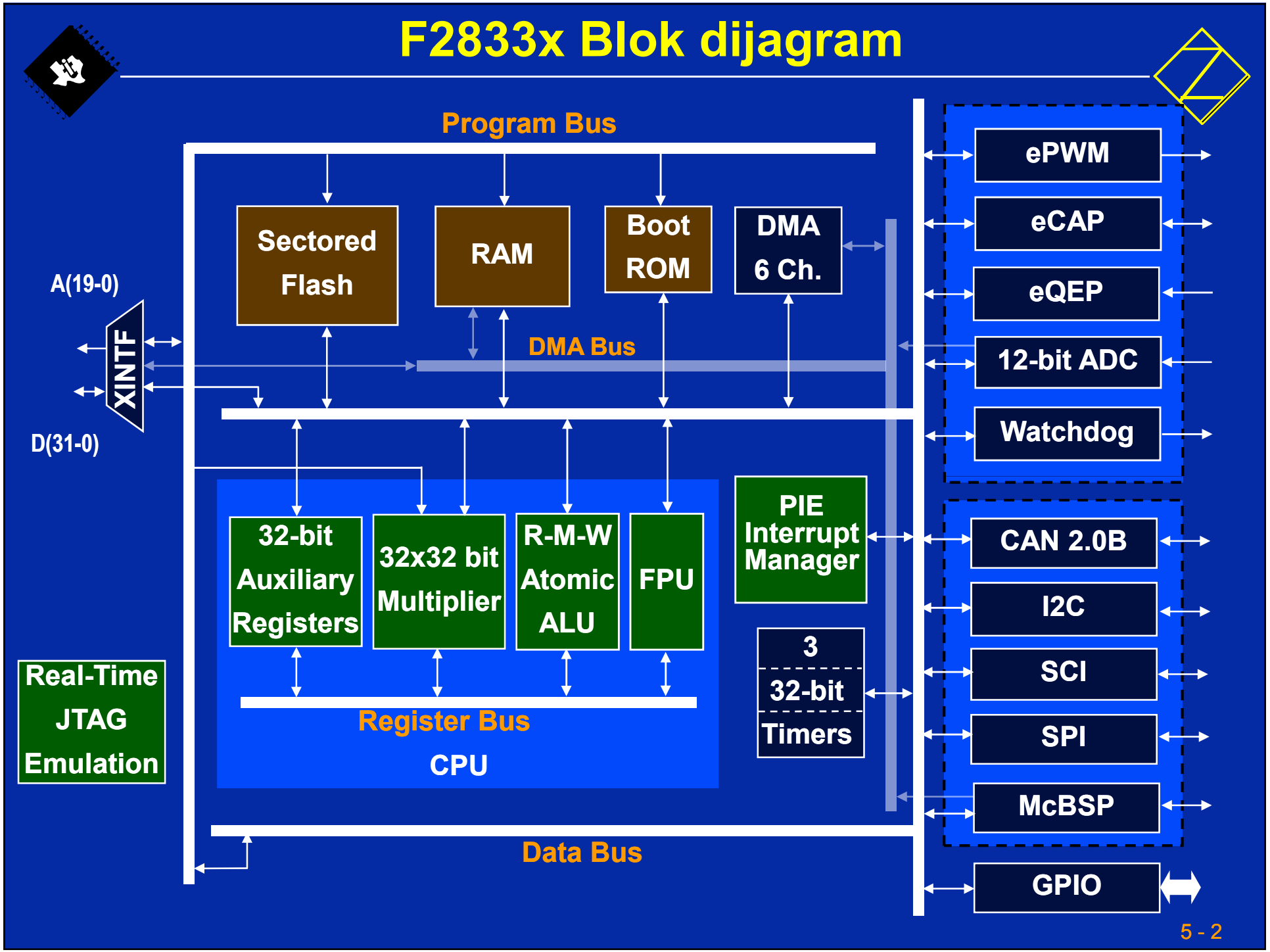
Modul 5: Digitalni Ulaz / Izlaz

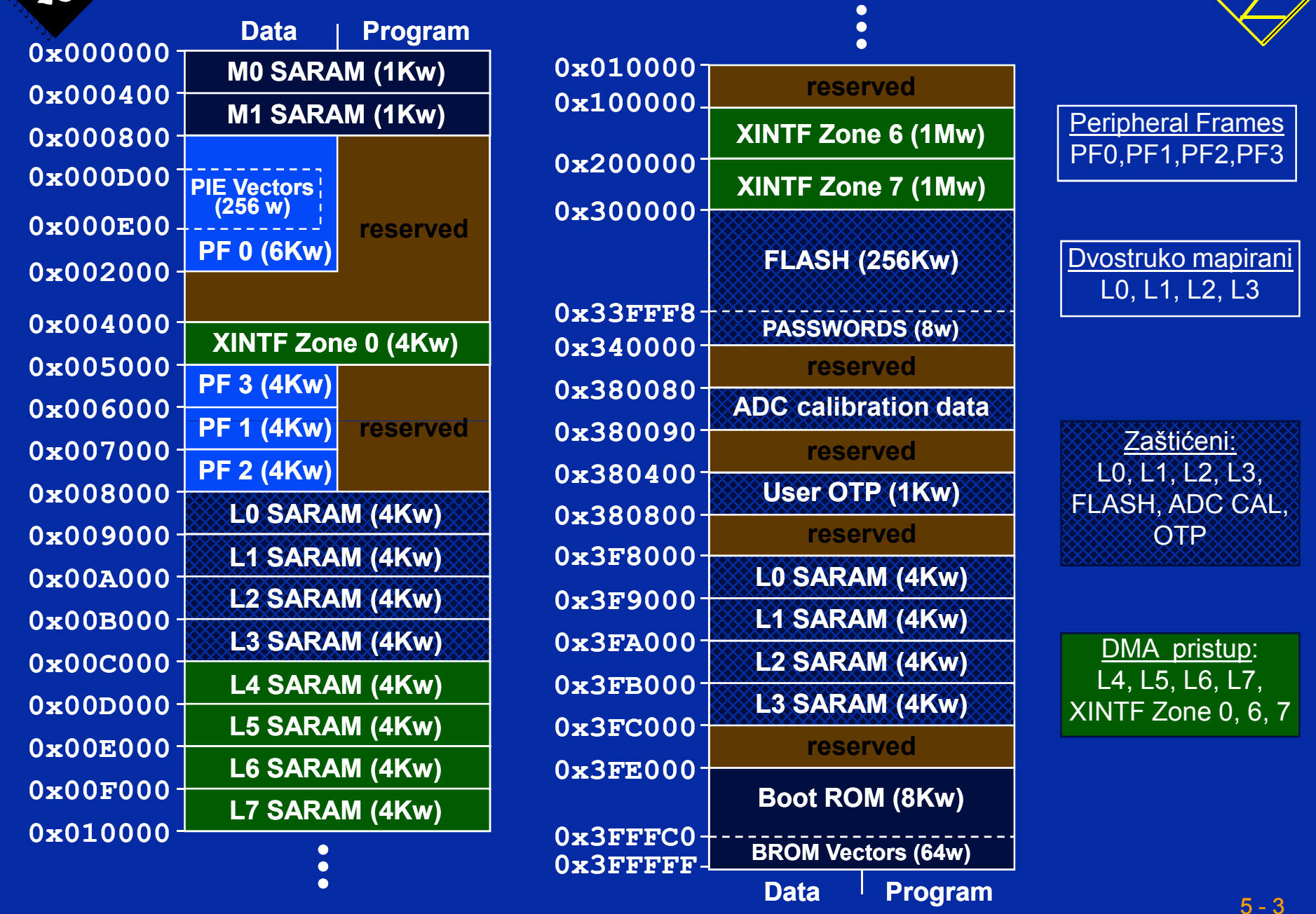
Digital Signal Controller
TMS320F2833x

Texas Instruments Incorporated

F2833x Blok dijagram



TMS320F2833x Memorijska mapa



Peripheral Frames
PF0,PF1,PF2,PF3

Dvostruko mapirani
L0, L1, L2, L3

Zaštićeni:
L0, L1, L2, L3, FLASH, ADC CAL, OTP

DMA pristup:
L4, L5, L6, L7, XINTF Zone 0, 6, 7

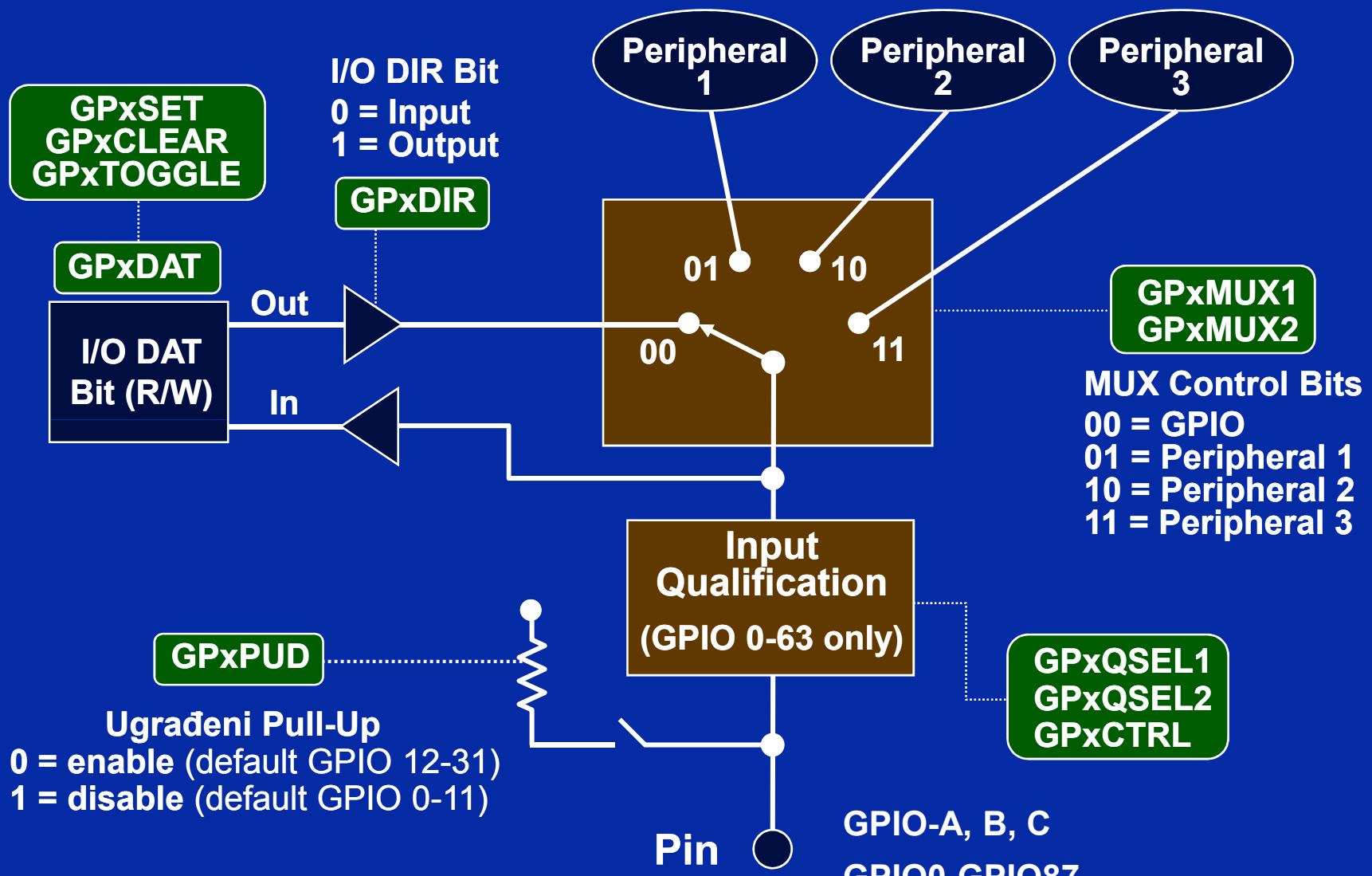
Mapiranje periferija

PF0:	PIE:	PIE Interrupt Enable and Control Registers plus PIE Vector Table
	Flash:	Flash Wait state Registers
	XINTF:	External Interface Registers
	DMA:	DMA Registers
	Timers:	CPU-Timers 0, 1, 2 Registers
	CSM:	Code Security Module KEY Registers
	ADC:	ADC Result registers (dual-mapped)
PF1:	eCAN:	eCAN Mailbox and Control Registers
	GPIO:	GPIO MUX Configuration and Control Registers
	ePWM:	Enhanced Pulse Width Modulator Module and Registers (dual mapped)
	eCAP:	Enhanced Capture Module and Registers
	eQEP:	Enhanced Quadrature Encoder Pulse Module and Registers

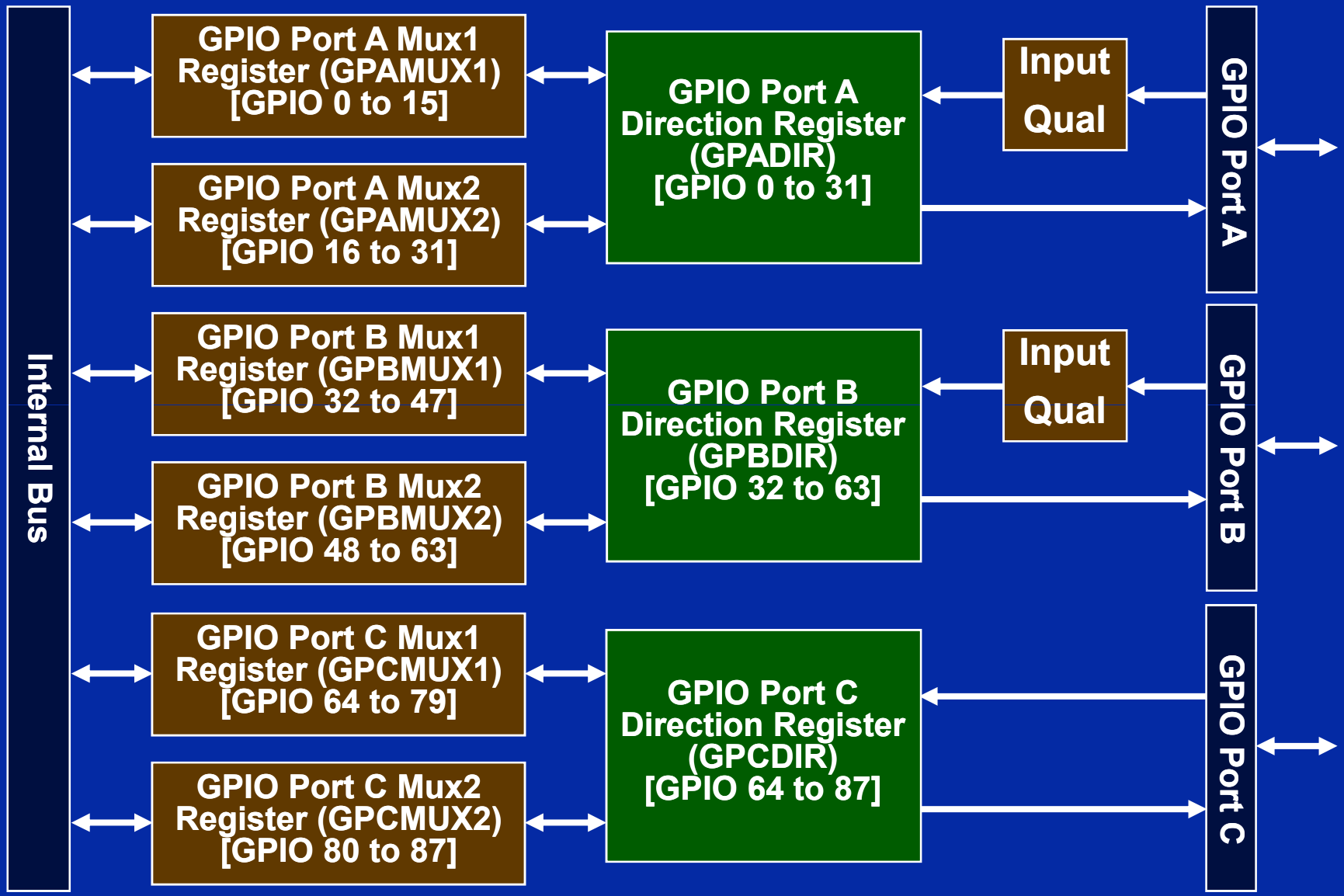
Mapiranje periferija

PF2:	SYS:	System Control Registers
	SCI:	Serial Communications Interface (SCI) Control and RX/TX Regis- ters
	SPI:	Serial Port Interface (SPI) Control and RX/TX Registers
	ADC:	ADC Status, Control, and Result Register
	I2C:	Inter-Integrated Circuit Module and Registers
	XINT:	External Interrupt Registers
PF3:	McBSP:	Multichannel Buffered Serial Port Registers
	ePWM:	Enhanced Pulse Width Modulator Module and Registers (dual mapped

F2833x GPIO blok dijagram veze pinova



Grupisanje GPIO F2833x



Brisanje linije GPIO5: `GpioDataRegs.GPACLEAR.bit.GPIO5 =1`

F2833x GPIO dodela funkcije pinovima (*assignment*)

GPIO - Multipleks registar GPAMUX1

GPAMUX1 - Bits	00	01	10	11
1,0	GPIO0	EPWM1A	-	-
3,2	GPIO1	EPWM1B	ECAP6	MFSRB
5,4	GPIO2	EPWM2A	-	-
7,6	GPIO3	EPWM2B	ECAP5	MCLKRB
9,8	GPIO4	EPWM3A	-	-
11,10	GPIO5	EPWM3B	MFSRA	ECAP1
13,12	GPIO6	EPWM4A	EPWMSYNCI	EPWMSYNC0
15,14	GPIO7	EPWM4B	MCLKRA	ECAP2
17,16	GPIO8	EPWM5A	CANTXB	/ADCSOCA0
19,18	GPIO9	EPWM5B	SCITXDB	ECAP3
21,20	GPIO10	EPWM6A	CANRXB	/ADCSOCB0
23,22	GPIO11	EPWM6B	SCIRXDB	ECAP4
25,24	GPIO12	/TZ1	CANTXB	SPISIMOB
27,26	GPIO13	/TZ2	CANRXB	SPISOMIB
29,28	GPIO14	/TZ3_/XHOLD	SCITXDB	SPICLKB
31,30	GPIO15	/TZ4_/XHOLDA	SCIRXDB	/SPISTEB

F2833x GPIO dodela funkcije pinovima (*assignment*)

GPIO - Multipleks registar GPAMUX2

GPAMUX2 - Bits	00	01	10	11
1,0	GPIO16	SPISIMOA	CANTXB	/TZ5
3,2	GPIO17	SPISOMIA	CANRXB	/TZ6
5,4	GPIO18	SPICLKA	SCITXDB	CANRXA
7,6	GPIO19	/SPISTEA	SCIRXDB	CANTXA
9,8	GPIO20	EQEP1A	MDXA	CANTXB
11,10	GPIO21	EQEP1B	MDRA	CANRXB
13,12	GPIO22	EQEP1S	MCLKXA	SCITXDB
15,14	GPIO23	EQEP1I	MFSXA	SCIRXDB
17,16	GPIO24	ECAP1	EQEP2A	MDXB
19,18	GPIO25	ECAP2	EQEP2B	MDRB
21,20	GPIO26	ECAP3	EQEP2I	MCLKXB
23,22	GPIO27	ECAP4	EQEP2S	MFSXB
25,24	GPIO28	SCIRXDA	/XZCS6	/XZCS6
27,26	GPIO29	SCITXDA	XA19	XA19
29,28	GPIO30	CANRXA	XA18	XA18
31,30	GPIO31	CANTXA	XA17	XA17

F2833x GPIO dodela funkcije pinovima (*assignment*)

GPIO - B Multipleks registar GPBMUX1

GPBMUX1 - Bits	00	01	10	11
1,0	GPIO32	SDAA	EPWMSYNCI	/ADCSOCA0
3,2	GPIO33	SCLA	EPWMSYNCO	/ADCSOCB0
5,4	GPIO34	ECAP1	XREADY	XREADY
7,6	GPIO35	SCITXDA	XR/W	XR/W
9,8	GPIO36	SCIRXDA	/XZCS0	/XZCS0
11,10	GPIO37	ECAP2	/XZCS7	/XZCS7
13,12	GPIO38	-	/XWE0	/XWE0
15,14	GPIO39	-	XA16	XA16
17,16	GPIO40	-	XA0/XWE1	XA0/XWE1
19,18	GPIO41	-	XA1	XA1
21,20	GPIO42	-	XA2	XA2
23,22	GPIO43	-	XA3	XA3
25,24	GPIO44	-	XA4	XA4
27,26	GPIO45	-	XA5	XA6
29,28	GPIO46	-	XA6	XA6
31,30	GPIO47	-	XA7	XA7

F2833x GPIO dodela funkcije pinovima (*assignment*)

GPIO - B Multipleks registar GPBMUX2

GPBMUX2 - Bits	00	01	10	11
1,0	GPIO48	ECAP5	XD31	XD31
3,2	GPIO49	ECAP6	XD30	XD30
5,4	GPIO50	EQEP1A	XD29	XD29
7,6	GPIO51	EQEP1B	XD28	XD28
9,8	GPIO52	EQEP1S	XD27	XD27
11,10	GPIO53	EQEP1I	XD26	XD26
13,12	GPIO54	SPISIMOA	XD25	XD25
15,14	GPIO55	SPISOMIA	XD24	XD24
17,16	GPIO56	SPICLKA	XD23	XD23
19,18	GPIO57	/SPISTEA	XD22	XD22
21,20	GPIO58	MCLKRA	XD21	XD21
23,22	GPIO59	MFSRA	XD20	XD20
25,24	GPIO60	MCLKRB	XD19	XD19
27,26	GPIO61	MFSRB	XD18	XD18
29,28	GPIO62	SCIRXDC	XD17	XD17
31,30	GPIO63	SCITXDC	XD16	XD16

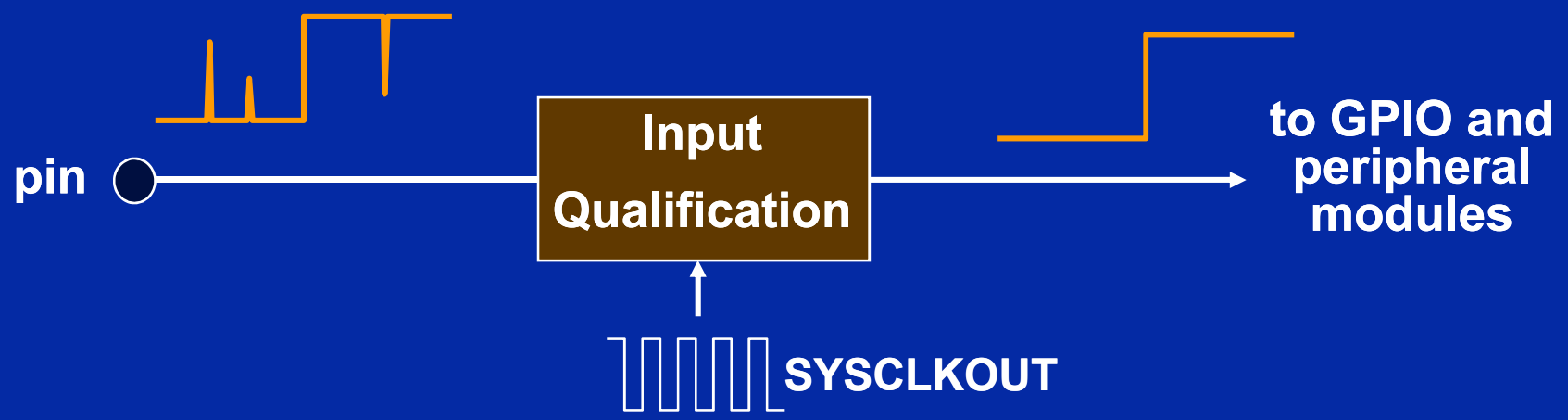
F2833x GPIO dodela funkcije pinovima (*assignment*)

GPIO - C Multipleks registar

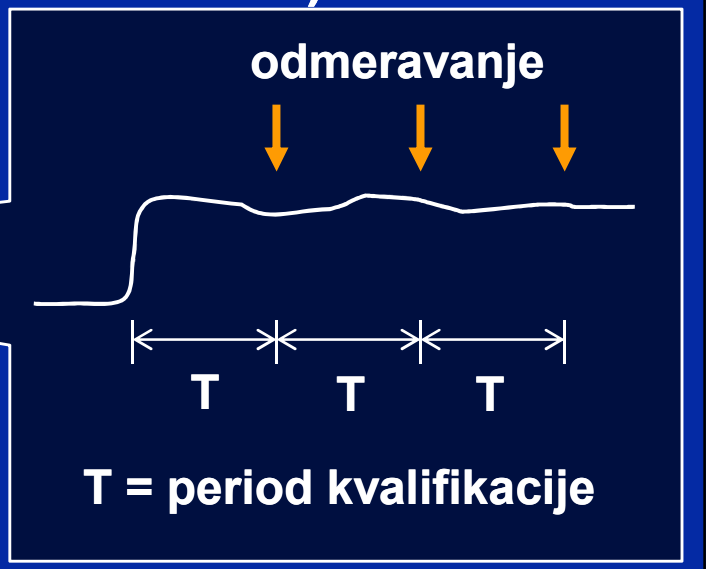
GPCMUX1 - Bits	00 or 01	10 or 11
1,0	GPIO64	XD15
3,2	GPIO65	XD14
5,4	GPIO66	XD13
7,6	GPIO67	XD12
9,8	GPIO68	XD11
11,10	GPIO69	XD10
13,12	GPIO70	XD9
15,14	GPIO71	XD8
17,16	GPIO72	XD7
19,18	GPIO73	XD6
21,20	GPIO74	XD5
23,22	GPIO75	XD4
25,24	GPIO76	XD3
27,26	GPIO77	XD2
29,28	GPIO78	XD1
31,30	GPIO79	XD0

GPCMUX2 - Bits	00 or 01	10 or 11
1,0	GPIO80	XA8
3,2	GPIO81	XA9
5,4	GPIO82	XA10
7,6	GPIO83	XA11
9,8	GPIO84	XA12
11,10	GPIO85	XA13
13,12	GPIO86	XA14
15,14	GPIO87	XA15
17,16	-	-
19,18	-	-
21,20	-	-
23,22	-	-
25,24	-	-
27,26	-	-
29,28	-	-
31,30	-	-

F2833x GPIO kvalifikacija ulaza



- Funkcija NF filtra za ulazni signal sa šumovima
- Kvalifikacija na portovima A & B (GPIO 0 - 63)
- Individualna selekcija za svaki pin
  - sync to SYCLKOUT only
  - qualify 3 samples
  - qualify 6 samples
  - Bez kvalifikacije (za periferije)
- Port C pinovi samo kao ‘sync to SYSCLKOUT’



F2833x GPIO Input Qualification Registers

GPAQSEL1 / GPAQSEL2 / GPBQSEL1 / GPBQSEL2

00 = sync to SYSCLKOUT only
01 = qual to 3 samples
10 = qual to 6 samples
11 = no sync or qual (for peripheral only; GPIO same as 00)

GPACTRL / GPBCTRL – perioda odmeravanja

B:	GPIO63-56	GPIO55-48	GPIO47-40	GPIO39-32
A:	GPIO31-24	GPIO23-16	GPIO15-8	GPIO7-0

0x00	no qualification (SYNC to SYSCLKOUT)
0x01	QUALPRD = $T_{SYSCLKOUT}$ * 2
0x02	QUALPRD = $T_{SYSCLKOUT}$ * 4
…	… …
0xFF	QUALPRD = $T_{SYSCLKOUT}$ * 510

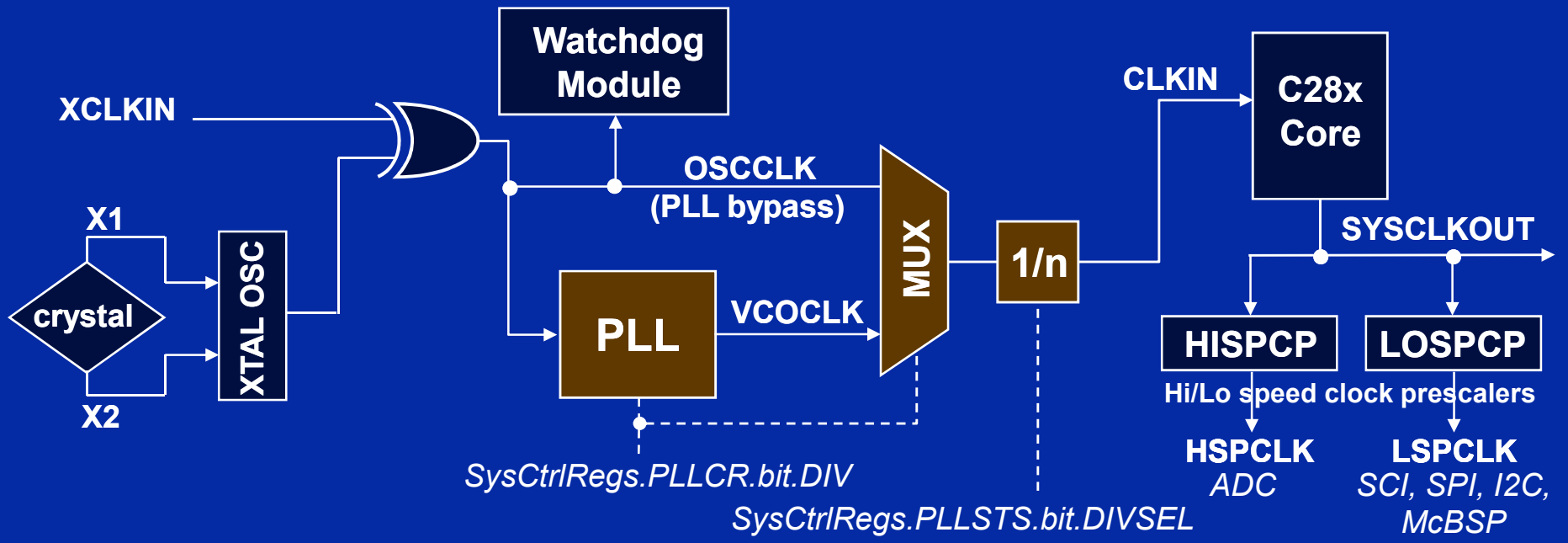
C2833x GPIO Kontrolni registri

Register	Description
GPACTRL	GPIO A Control Register [GPIO 0 – 31]
GPAQSEL1	GPIO A Qualifier Select 1 Register [GPIO 0 – 15]
GPAQSEL2	GPIO A Qualifier Select 2 Register [GPIO 16 – 31]
GPAMUX1	GPIO A Mux1 Register [GPIO 0 – 15]
GPAMUX2	GPIO A Mux2 Register [GPIO 16 – 31]
GPADIR	GPIO A Direction Register [GPIO 0 – 31]
GPAPUD	GPIO A Pull-Up Disable Register [GPIO 0 – 31]
GPBCTRL	GPIO B Control Register [GPIO 32 – 63]
GPBQSEL1	GPIO B Qualifier Select 1 Register [GPIO 32 – 47]
GPBQSEL2	GPIO B Qualifier Select 2 Register [GPIO 48 – 63]
GPBMUX1	GPIO B Mux1 Register [GPIO 32 – 47]
GPBMUX2	GPIO B Mux2 Register [GPIO 48 – 63]
GPBDIR	GPIO B Direction Register [GPIO 32 – 63]
GPBPUD	GPIO B Pull-Up Disable Register [GPIO 32 – 63]
GPCMUX1	GPIO C Mux1 Register [GPIO 64 – 79]
GPCMUX2	GPIO C Mux2 Register [GPIO 80 – 87]
GPCDIR	GPIO C Direction Register [GPIO 64 – 87]
GPCPUD	GPIO C Pull-Up Disable Register [GPIO 64 – 87]

C2833x GPIO *Data* registri

Register	Description
GPADAT	GPIO A Data Register [GPIO 0 – 31]
GPASET	GPIO A Data Set Register [GPIO 0 – 31]
GPACLEAR	GPIO A Data Clear Register [GPIO 0 – 31]
GPATOGGLE	GPIO A Data Toggle [GPIO 0 – 31]
GPBDAT	GPIO B Data Register [GPIO 32 – 63]
GPBSET	GPIO B Data Set Register [GPIO 32 – 63]
GPBCLEAR	GPIO B Data Clear Register [GPIO 32 – 63]
GPBTOGGLE	GPIO B Data Toggle [GPIO 32 – 63]
GPCDAT	GPIO C Data Register [GPIO 64 – 87]
GPCSET	GPIO C Data Set Register [GPIO 64 – 87]
GPCCLEAR	GPIO C Data Clear Register [GPIO 64 – 87]
GPCTOGGLE	GPIO C Data Toggle [GPIO 64 – 87]

F2833x Clock Module



Sve druge periferije se taktuju sa SYSCLKOUT

DIVSEL	n
0x	/4 *
10	/2
11	/1

*** default**

Napomena:

režim "/1" je moguće koristiti sako kada se PLL ne koristi (PLL bypass)

DIV	CLKIN
0 0 0 0	OSCCLK / n * (PLL bypass)
0 0 0 1	OSCCLK x 1 / n
0 0 1 0	OSCCLK x 2 / n
0 0 1 1	OSCCLK x 3 / n
0 1 0 0	OSCCLK x 4 / n
0 1 0 1	OSCCLK x 5 / n
0 1 1 0	OSCCLK x 6 / n
0 1 1 1	OSCCLK x 7 / n
1 0 0 0	OSCCLK x 8 / n
1 0 0 1	OSCCLK x 9 / n
1 0 1 0	OSCCLK x 10 / n

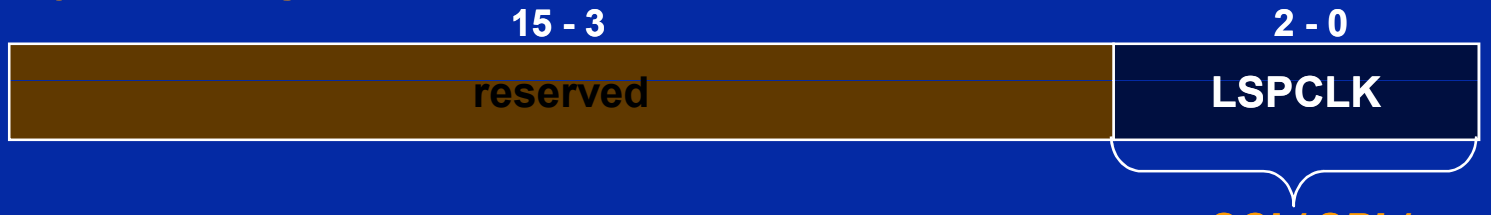
Kolo za detekciju odsustva takta

PLL prelazi u "limp" režim (1-4 MHz) ako nema ulaznog takt signala nakon što je PLL ušo u singronizaciju.

F2833x Delitelji takta

SysCtrlRegs.HISPCP

SysCtrlRegs.LOSPCP



H/LSPCLK	Peripheral Clock Frequency
0 0 0	SYSCLKOUT / 1
0 0 1	SYSCLKOUT / 2 (default HISPCP)
0 1 0	SYSCLKOUT / 4 (default LOSPCP)
0 1 1	SYSCLKOUT / 6
1 0 0	SYSCLKOUT / 8
1 0 1	SYSCLKOUT / 10
1 1 0	SYSCLKOUT / 12
1 1 1	SYSCLKOUT / 14

Napomena:

Sve druge periferije Taktuju se sa SYSCLKOUT

F2833x Kontrolna jedinica za distribuciju takta

SysCtrlRegs.PCLKCR0

15	14	13	12	11	10	9	8
ECANB ENCLK	ECANA ENCLK	MA ENCLK	MB ENCLK	SCIB ENCLK	SCIA ENCLK	reserved	SPIA ENCLK
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
reserved	reserved	SCIC ENCLK	I2CA ENCLK	ADC ENCLK	TBCLK SYNC	reserved	reserved

SysCtrlRegs.PCLKCR1

15	14	13	12	11	10	9	8
EQEP2 ENCLK	EQEP1 ENCLK	ECAP6 ENCLK	ECAP5 ENCLK	ECAP4 ENCLK	ECAP3 ENCLK	ECAP2 ENCLK	ECAP1 ENCLK
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
reserved	reserved	EPWM6 ENCLK	EPWM5 ENCLK	EPWM4 ENCLK	EPWM3 ENCLK	EPWM2 ENCLK	EPWM1 ENCLK

SysCtrlRegs.PCLKCR3

15 - 14	13	12	11	10	9	8	7 - 0
reserved	GPIOIN ENCLK	XINTF ENCLK	DMA ENCLK	CPUTIMER2 ENCLK	CPUTIMER1 ENCLK	CPUTIMER0 ENCLK	reserved

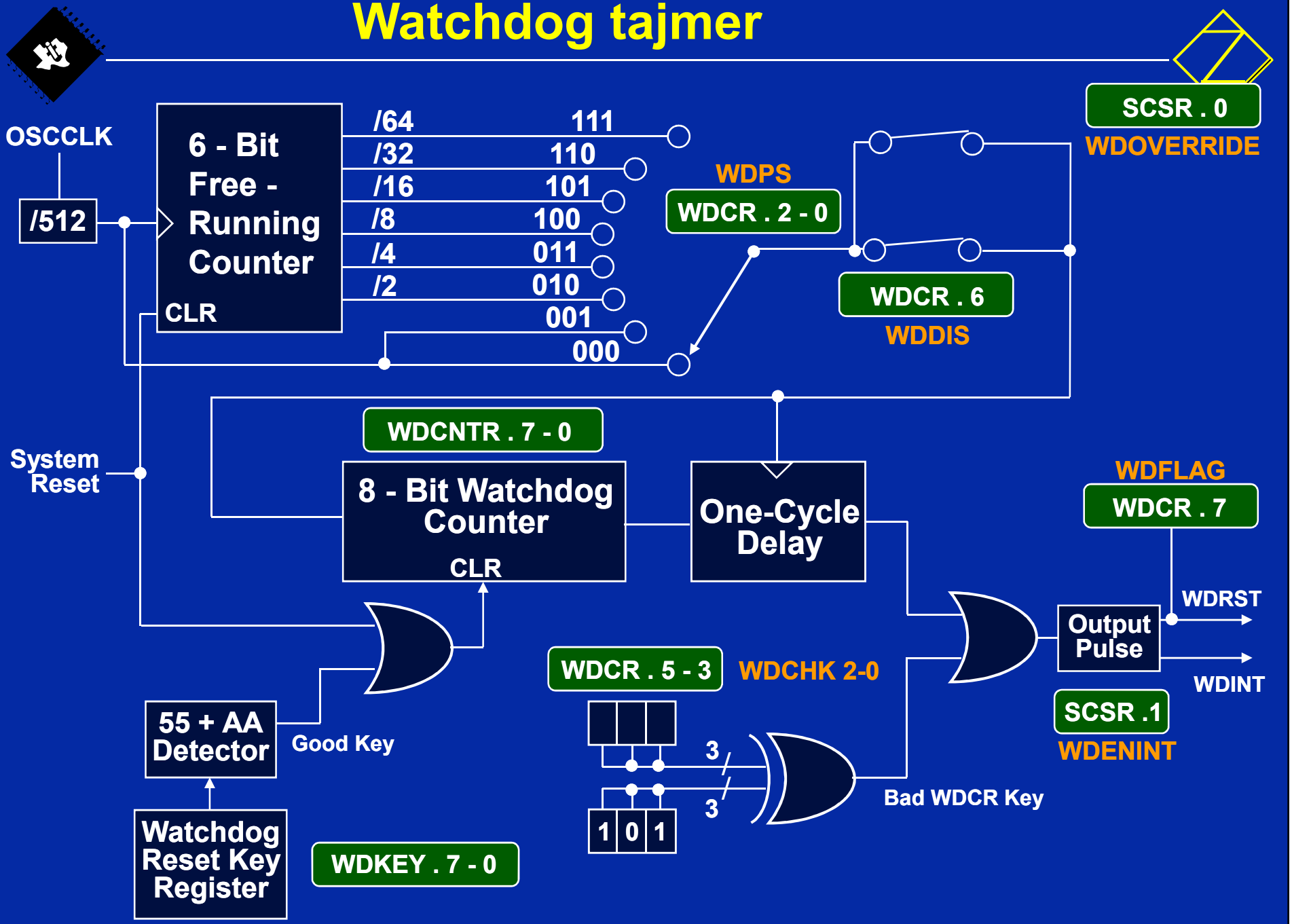
Module Enable Clock Bit

0 = disable (default) 1 = enable

Watchdog tajmer

- Resetuje F2833x ako CPU krahira
  - Watchdog brojač radi nezavisno od CPU
  - Ako dođe do premašenja brojača, javlja se reset ili prekid (moguće je izabrati)
  - CPU mora upisati korektan niz podataka (*key sequence*) da bi se brojač resetovao
- Watchdog mora biti servisiran ili zabranjen njegov rad 4.37ms nakon reseta (za slučaj da je 30 MHz OSCCLK)
- Oaj vremenski period odgovara izvršavanju 645000 instructija kada CPU radi na 150MHz!

Watchdog tajmer



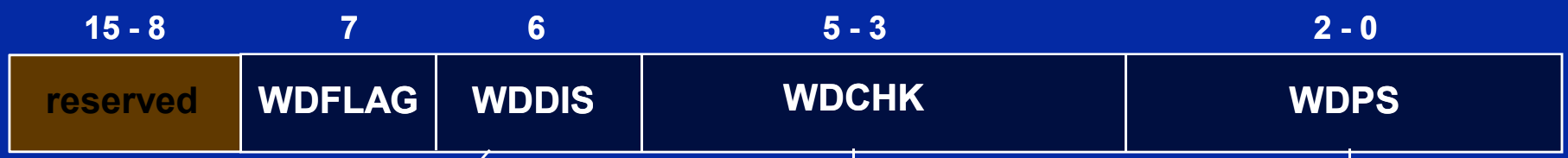
Watchdog Timer Control Register

Register: SysCtrlRegs.WDCR

WD Flag Bit

Postavlja se kada WD uzrokuje reset

- **Upis 1 briše ovaj bit**
- **Upis 0 nema efekta**



Watchdog Disable Bit

Upis 1 zabranjuje rad WD (Ima funkciju samo ako je WD OVERRIDE bit u SCSR = 1)

Logic Check Bits

Upis 101 ili trenutno resetovanje

WD Prescale Selection Bits

Resetovanje Watchdog-a

15 - 8	7 - 0
reserved	WDKEY

- WDKEY sekvenca upisa:
  - 0x55 – dozvola za upis sledeće reči 0xAA
  - 0xAA – brojač resetuje ako je reset dozvoljen
- Upis bilo koje vrednosti nema efekta
- Watchdog ne treba servisirati samo u ISR
  - Ako glavni program krahira, ali prekidni nastavlja da se izvršava watchdog neće resetovati CPU
  - Mogućnost stavljanja 0x55 WDKEY u glavni program, a 0xAA WDKEY u neku ISR;

WDKEY sekvence

Sequential Step	Value Written to WDKEY	Result
1	AAh	No action
2	AAh	No action
3	55h	WD counter enabled for reset on next AAh write
4	55h	WD counter enabled for reset on next AAh write
5	55h	WD counter enabled for reset on next AAh write
6	AAh	WD counter is reset
7	AAh	No action
8	55h	WD counter enabled for reset on next AAh write
9	AAh	WD counter is reset
10	55h	WD counter enabled for reset on next AAh write
11	23h	No effect; WD counter not reset on next AAh write
12	AAh	No action due to previous invalid value
13	55h	WD counter enabled for reset on next AAh write
14	AAh	WD counter is reset

System Control and Status Register

Register: SysCtrlRegs.SCSR

WD Override (protect bit)

Štiti WD od njegove zabrane

0 = WDDIS bit in WDCR nema efekta (WD ne može biti zabranjen)
1 = WDDIS bit in WDCR može zabraniti watchdog

- Ovo je *clear-only* bit (upis 1 za brisanje)
- The reset default of this bit is a 1

WD Interrupt Status (read only)

0 = active
1 = not active

WD Enable Interrupt

0 = WD generiše DSP reset
1 = WD generiše WDINT interrupt

Low Power Modes

Low Power Mode	CPU Logic Clock	Peripheral Logic Clock	Watchdog Clock	PLL / OSC
Normal Run	on	on	on	on
IDLE	off	on	on	on
STANDBY	off	off	on	on
HALT	off	off	off	off

Potrošnja u svakom režimu može se videti iz kataloga

Low Power Mode Control Register 0

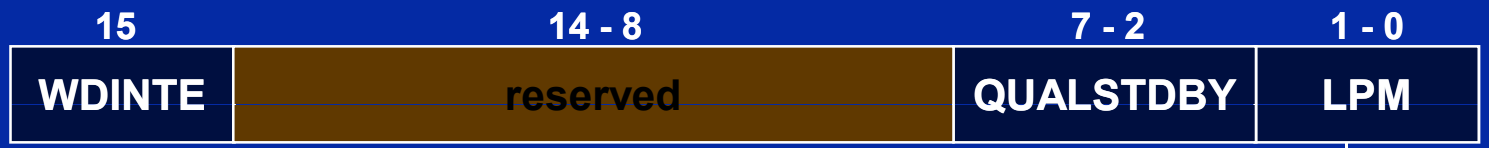
Registar: SysCtrlRegs.LPMCR0

Watchdog Interrupt izlaz kola iz STANDBY

0 = disable (default)
1 = enable

Izlaz iz STANDBY signalom GPIO (kvalifikacija*)

000000 = 2 OSCCLKs
000001 = 3 OSCCLKs
⋮ ⋮ ⋮
111111 = 65 OSCCLKS (default)



Izbor režima male potrošnje

00 = Idle (default)
01 = Standby
1x = Halt

Ulaz u režim male potrošnje

1. Postavljanje LPM bitova
2. Dozvola željenog izlaza - interapta
3. Izvršavanje IDLE instrukcije
4. Sekvenca ulaza u režim zavisi od LP režima

* QUALSTDBY kvalifikuje GPIO izlaz iz režima male potrošnje sabrano sa GPIO port kvalifikacijom.

Izlaz iz režima male potrošnje

Exit Interrupt / Low Power Mode	RESET or XNMI	GPIO Port A Signal	Watchdog Interrupt	Any Enabled Interrupt
IDLE	yes	yes	yes	yes
STANDBY	yes	yes	yes	no
HALT	yes	yes	no	no

Izbor GPIO linije za izlaz iz LP

Register: SysCtrlRegs.GPIOLPMSEL

31	30	29	28	27	26	25	24
GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

Wake device from HALT and STANDBY mode (GPIO Port A)

0 = disable (default)
1 = enable