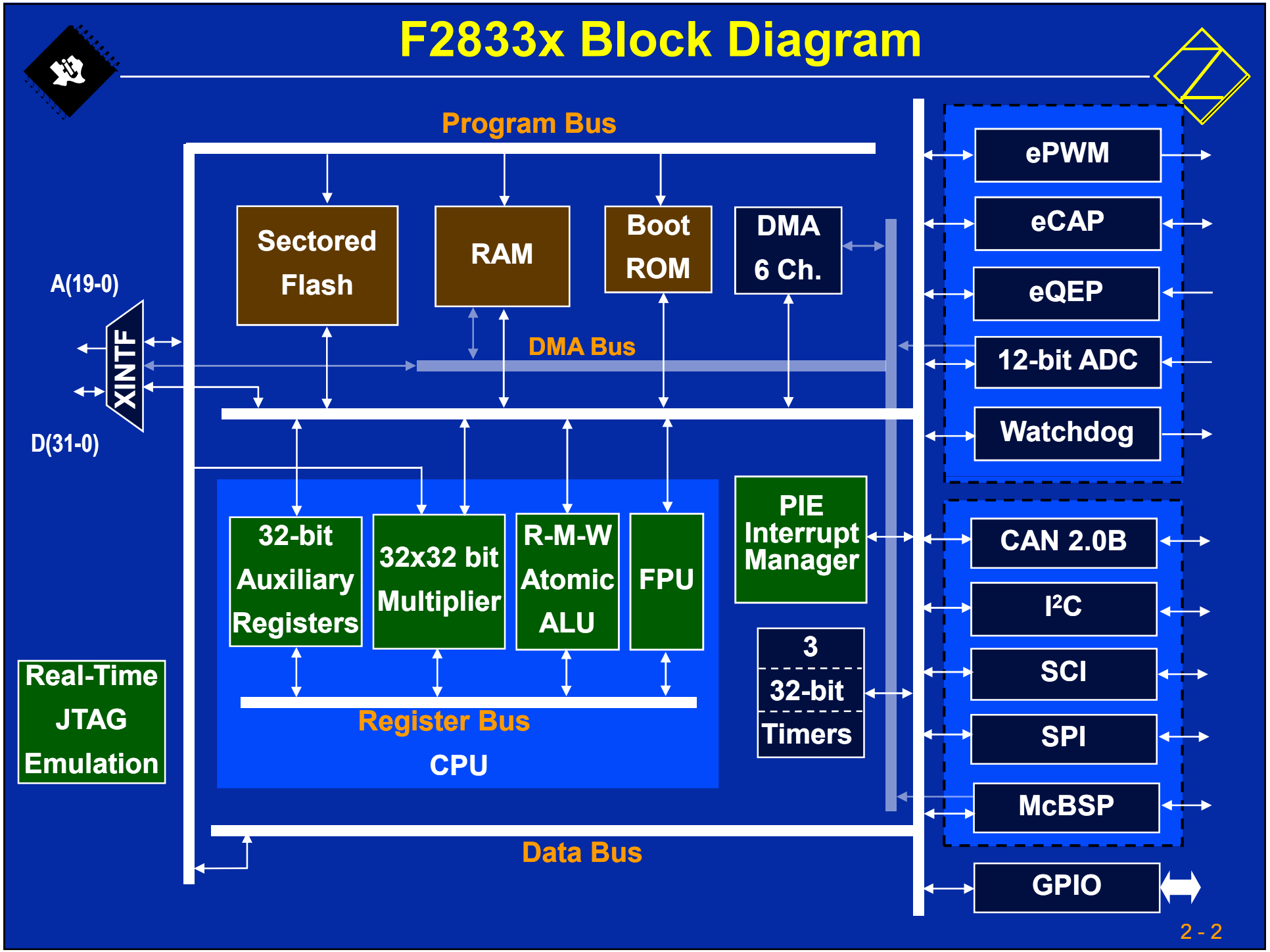
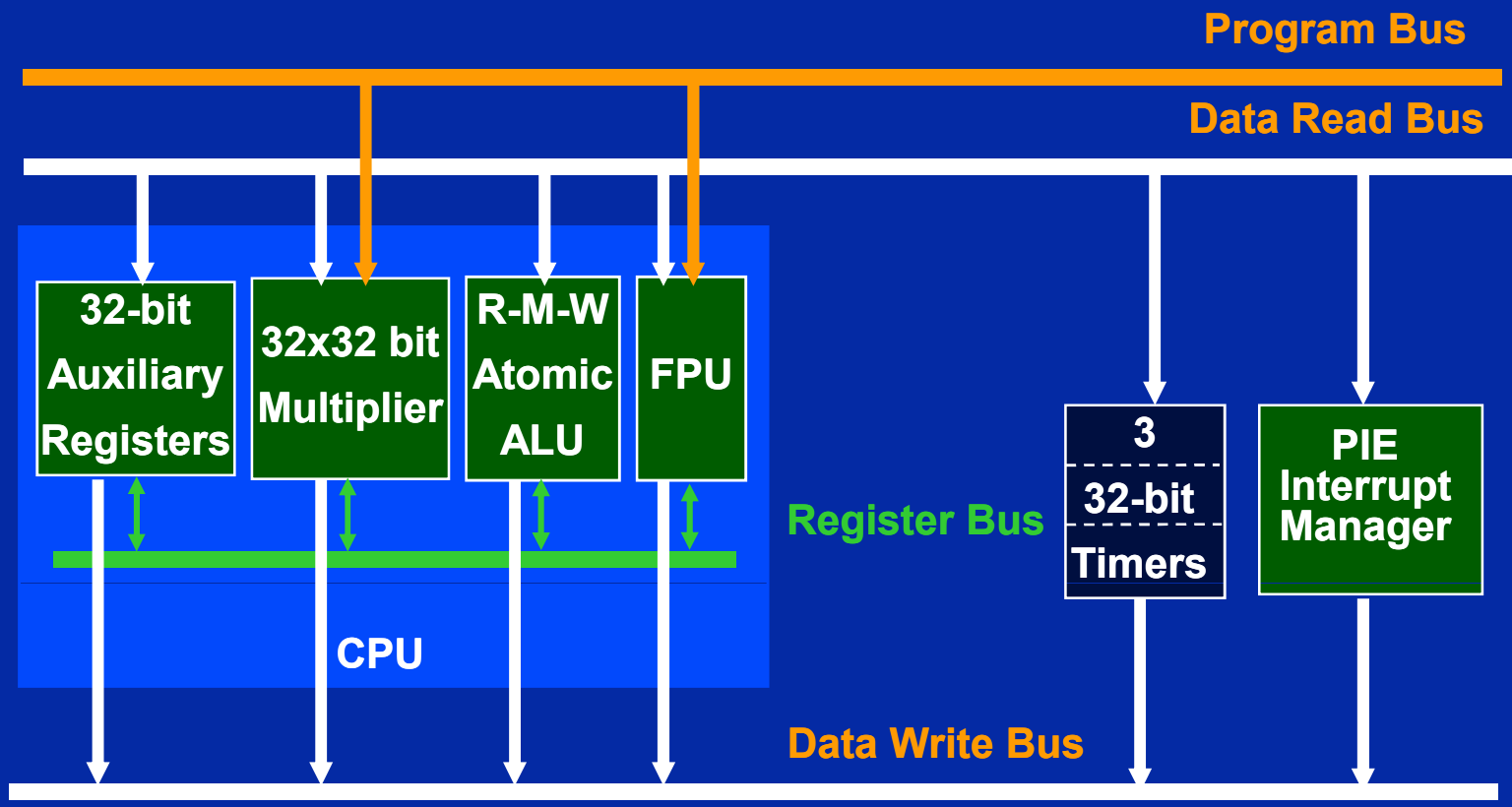
Digital Signal Controller
TMS320F28335

Texas Instruments Incorporated

F2833x Block Diagram



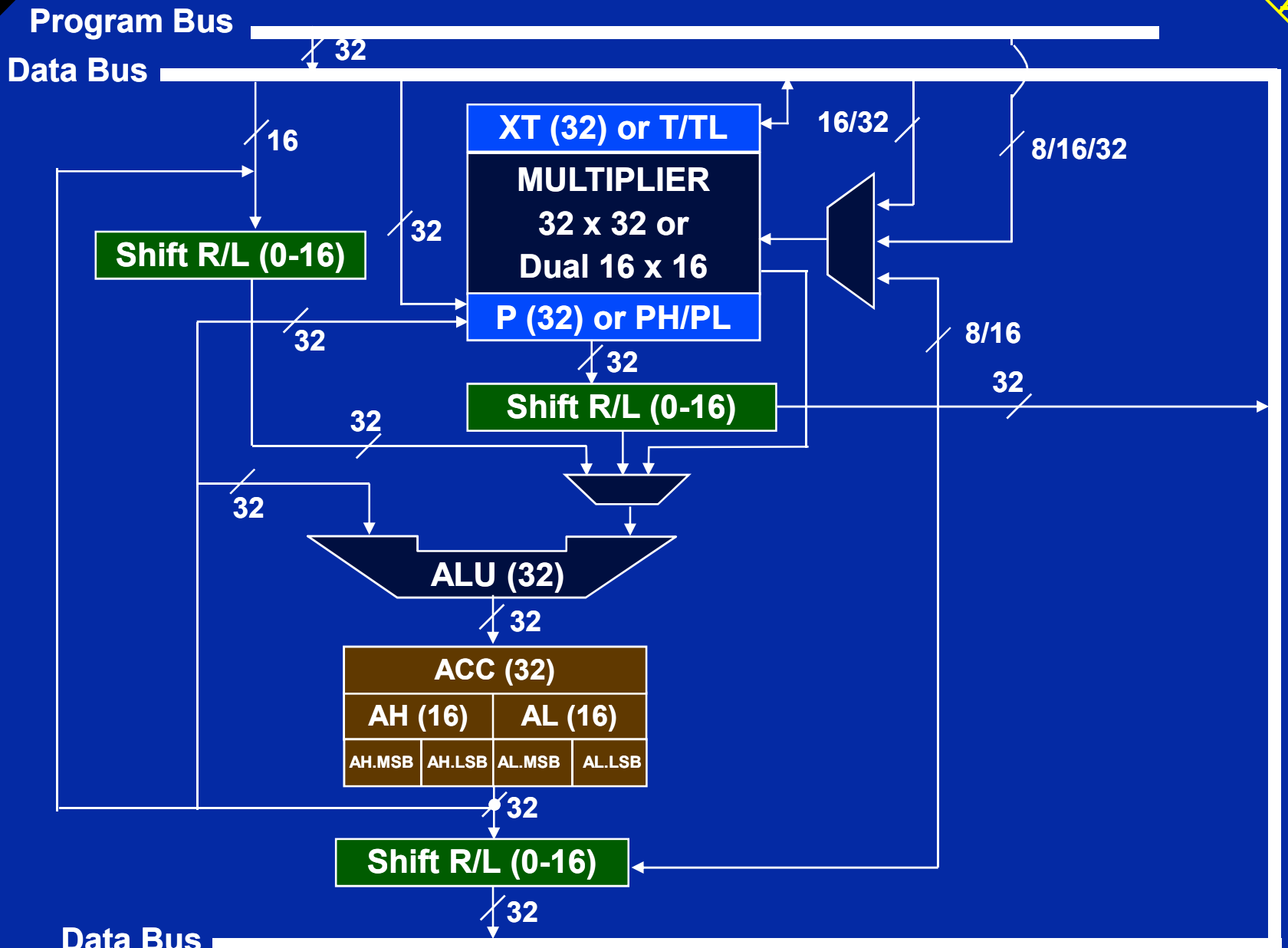
F2833x CPU



- 32-bit fixed and floating point DSP ; 32 x 32 bit fixed-point MAC
- Additional 32 x 32 bit hardware floating point unit
- Dual 16 x 16 single-cycle fixed-point MAC (DMAC)
- 32-/64-bit saturation
- Unique real-time debugging capabilities

Real-Time JTAG Emulation

F2833x Fixed Point Multiplier and ALU



F2833x Floating Point Unit FPU

32-bit Accumulator, Product, Temporary and 8 Auxiliary Registers

22-bit Program Counter Return PC

16-bit

Data Page Pointer
Stack Pointer

2 Status
Interrupt Enable
Interrupt Flag

Fixed Point

C28 Register Set

- ACC
- P
- XT
- XAR0
- XAR1
- XAR2
- XAR3
- XAR4
- XAR5
- XAR6
- XAR7
- PC
- RPC
- DP
- SP
- ST0
- ST1
- IER
- IFR
- DBGIER

Floating Point

FPU Register Set

- R0H
- R1H
- R2H
- R3H
- R4H
- R5H
- R6H
- R7H
- STF
- RB

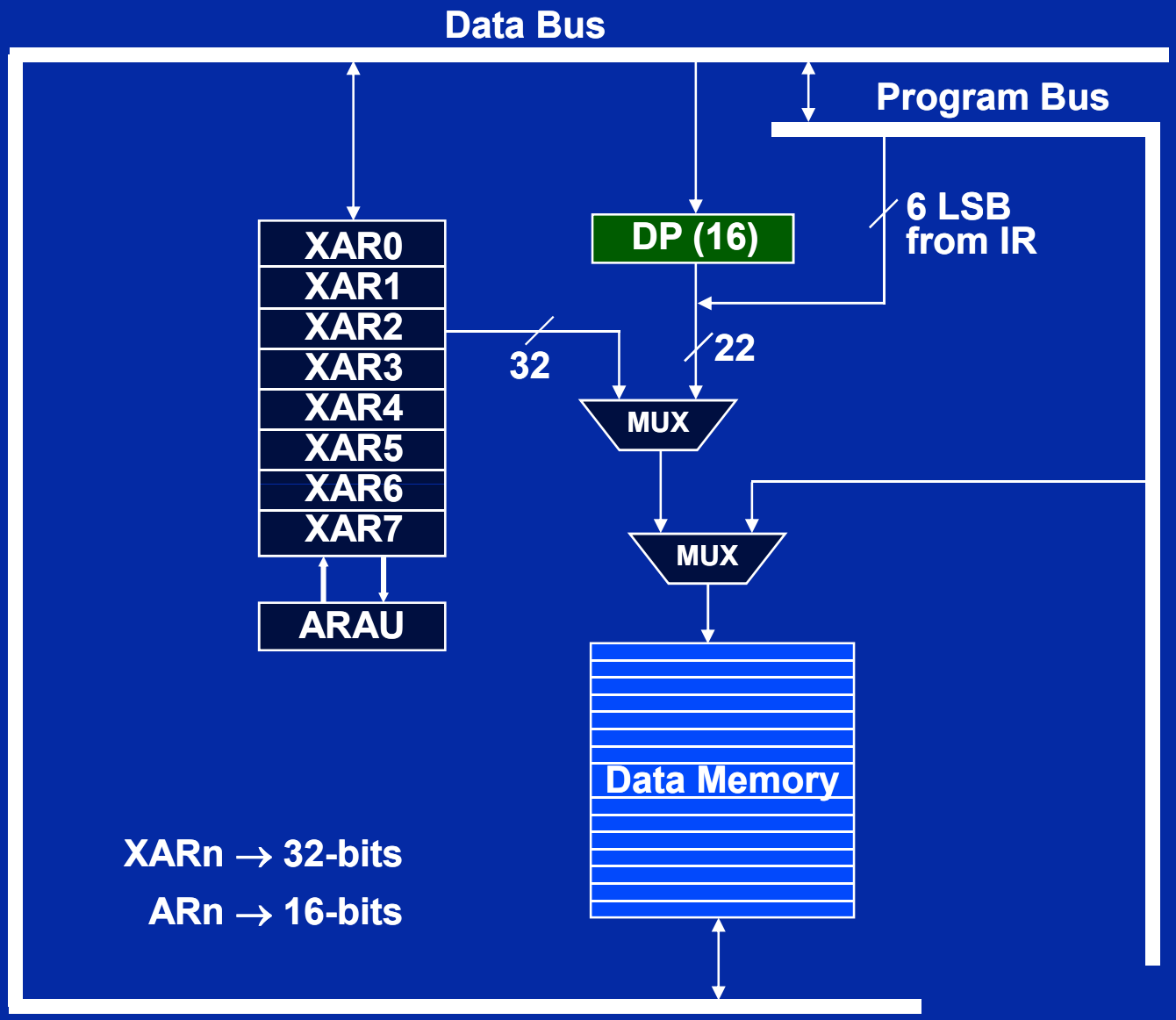
32-bit

8 FPU Result Registers

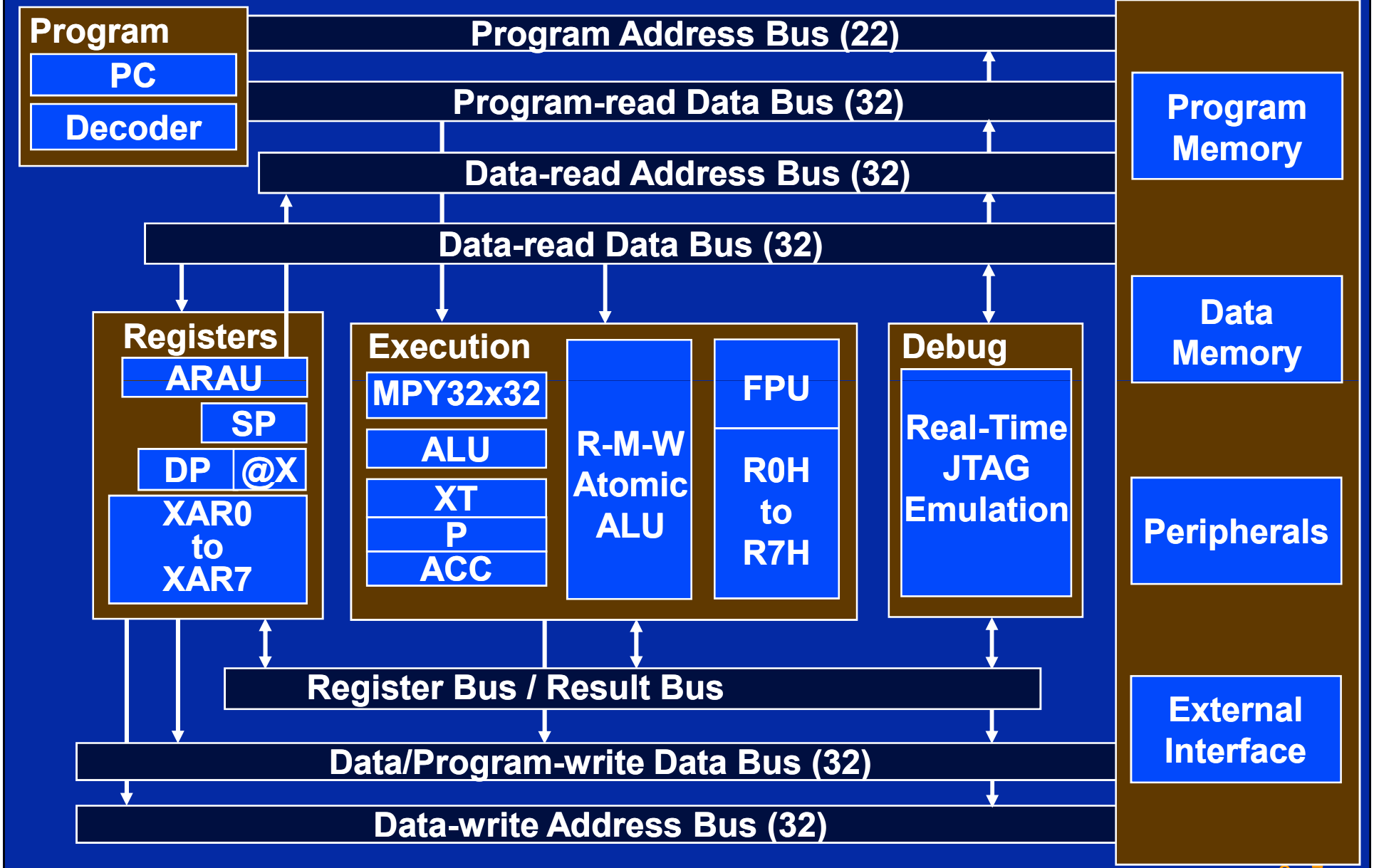
FPU Status Repeat Block

R0H – R7H And STF Are Shadowed For Fast Context Save And Restore

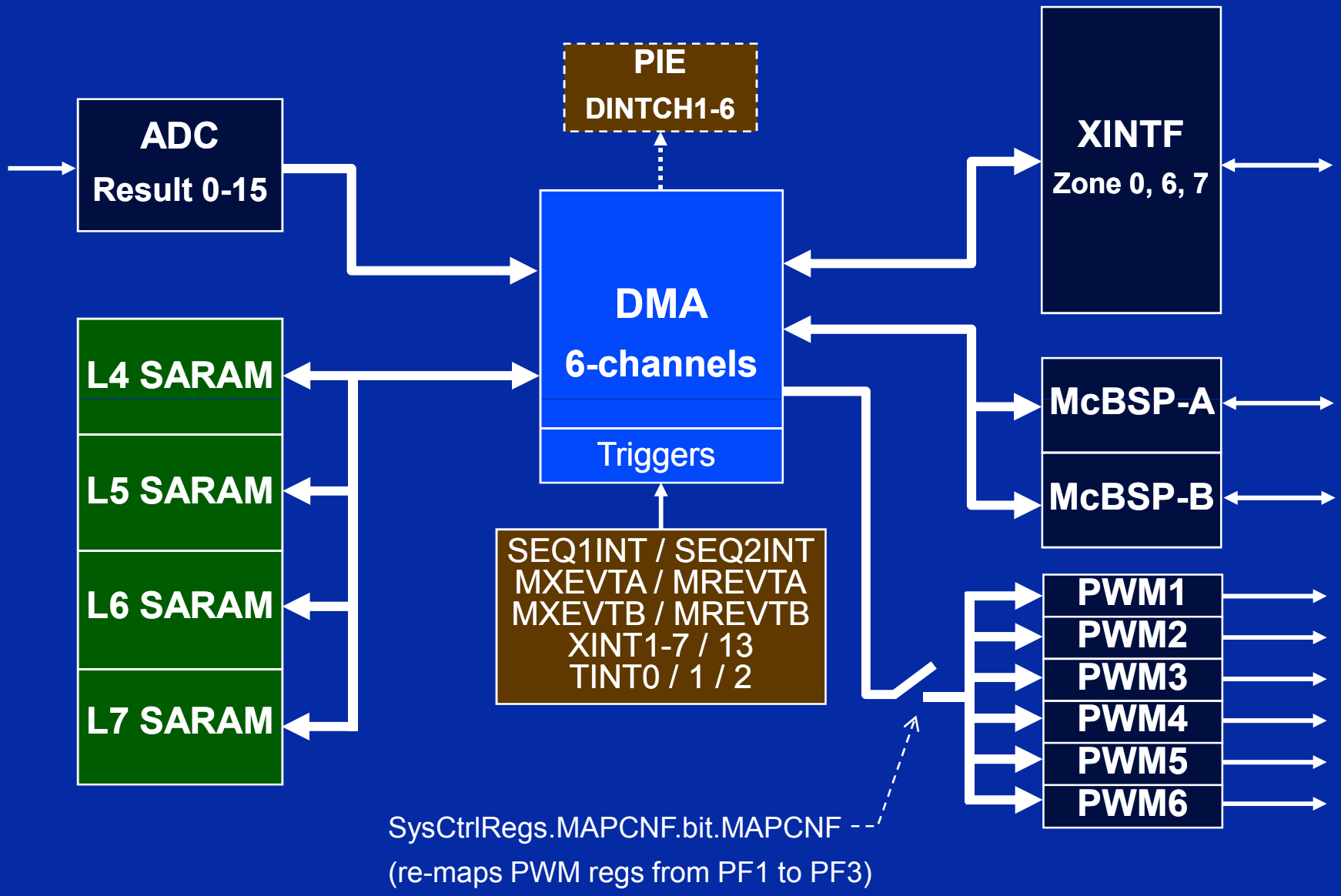
F2833x Pointer, DP and Memory



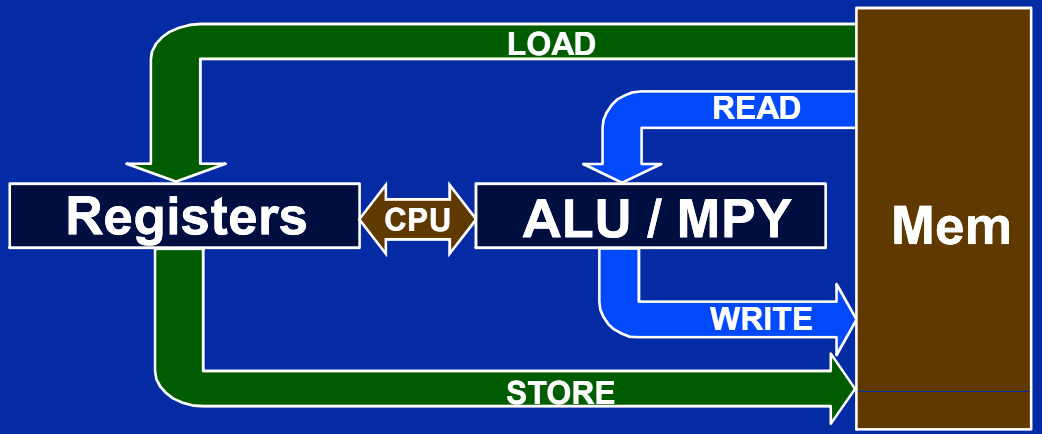
F2833x Internal Bus Structure



F2833x Direct Memory Access



F2833x Atomic Read/Modify/Write



- Atomic Instructions Benefits:
  - Simpler programming
  - Smaller, faster code
  - Uninterruptible (Atomic)
  - More efficient compiler

Standard Load/Store

```
DINT
MOV     AL,*XAR2
AND     AL,#1234h
MOV     *XAR2,AL
EINT
```

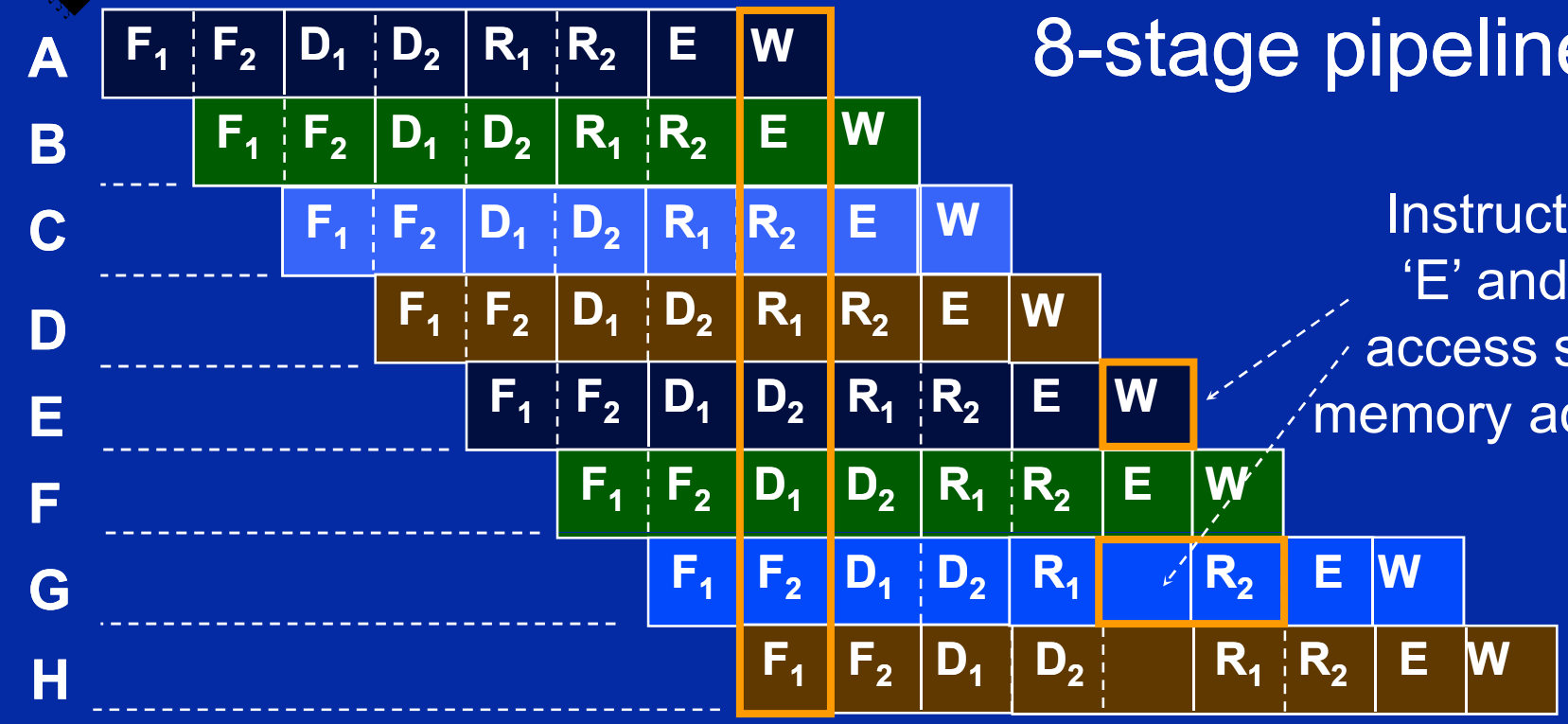
6 words / 6 cycles

Atomic Read/Modify/Write

```
AND    *XAR2,#1234h
```

2 words / 1 cycles

F2833x Pipeline



8-stage pipeline

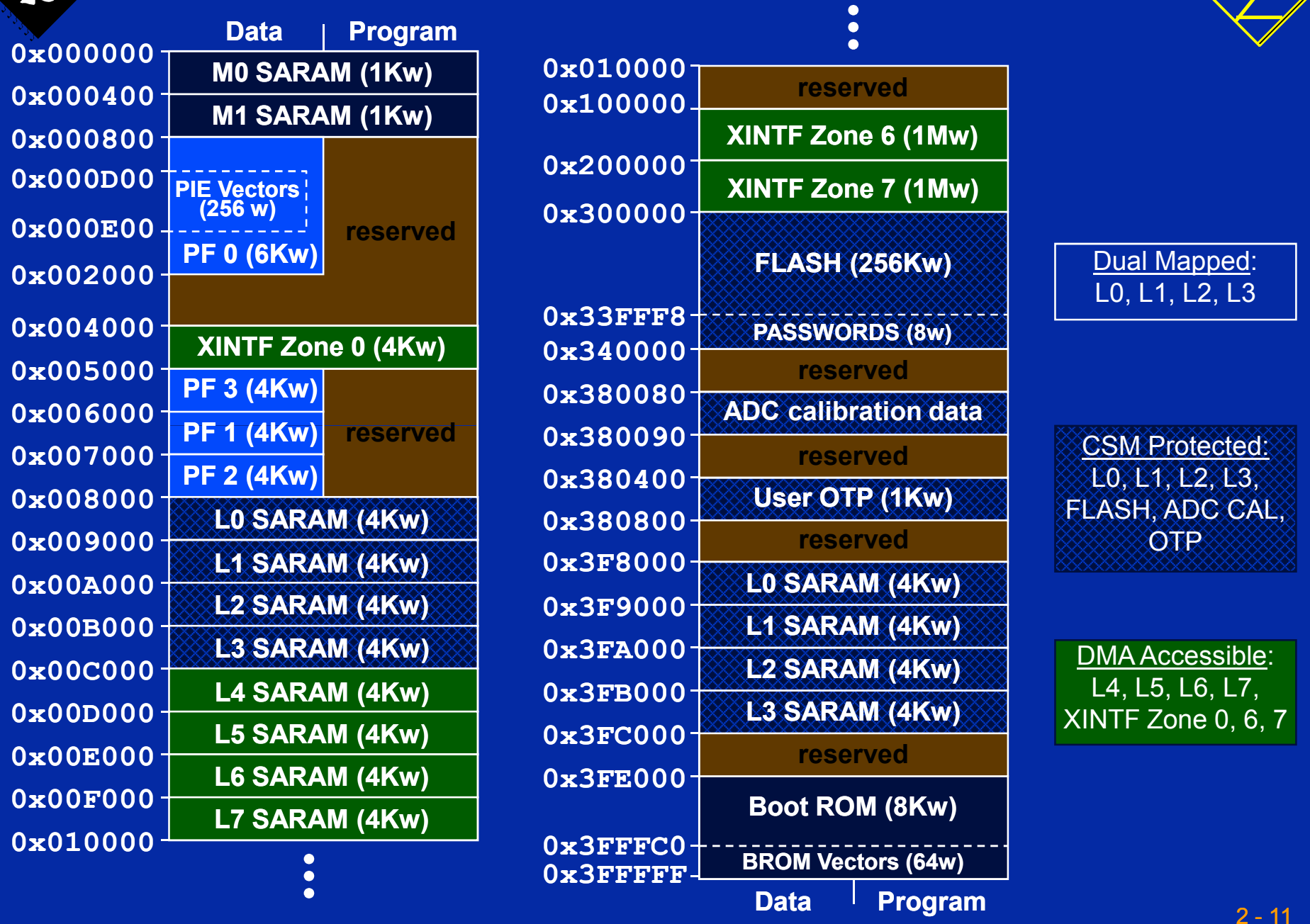
Instructions 'E' and 'G' access same memory address

F1: Instruction Address
F2: Instruction Content
D1: Decode Instruction
D2: Resolve Operand Addr
R1: Operand Address
R2: Get Operand
E: CPU doing "real" work
W: store content to memory

Protected Pipeline

- **Order of results are as written in source code**
- ***Programmer need not worry about the pipeline***

TMS320F2833x Memory Map



Dual Mapped:
L0, L1, L2, L3

CSM Protected:
L0, L1, L2, L3, FLASH, ADC CAL, OTP

DMA Accessible:
L4, L5, L6, L7, XINTF Zone 0, 6, 7

Code Security Module

- Prevents reverse engineering and protects valuable intellectual property

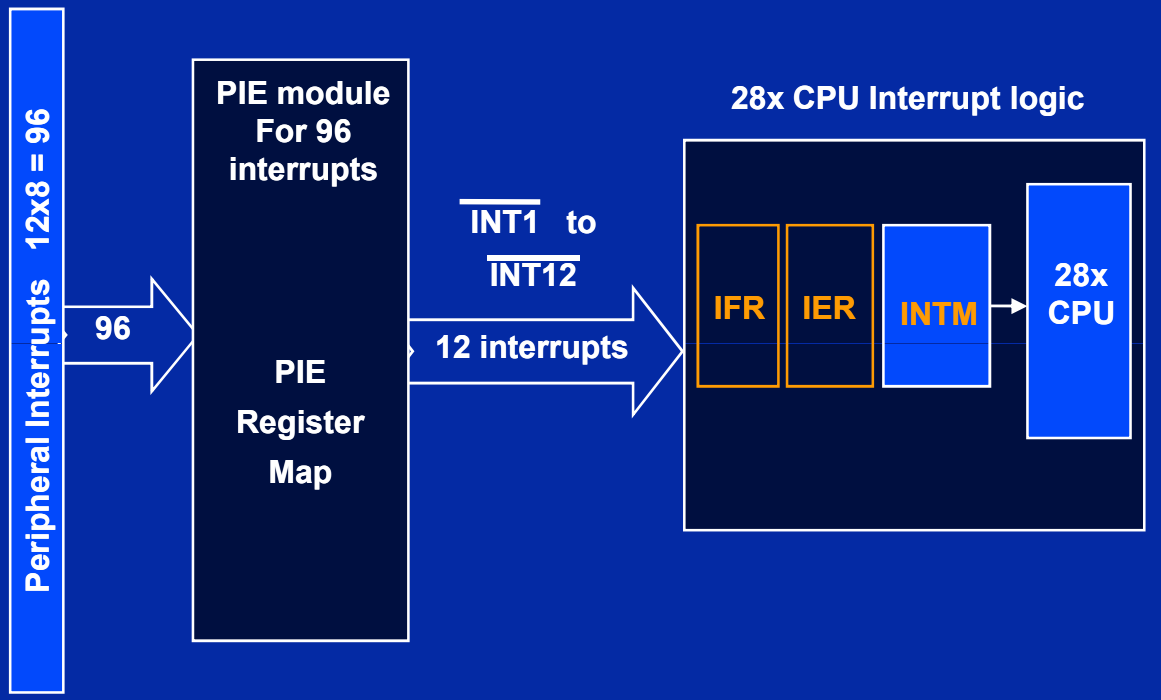
CSM Protected:
L0, L1, L2, L3,
FLASH, ADC CAL,
OTP

- 128-bit user defined password is stored in Flash
- 128-bits = 2^{128} = 3.4 x 10^{38} possible passwords
- To try 1 password every 2 cycles at 150 MHz, it would take at least 1.4 x 10^{23} years to try all possible combinations!

F2833x Fast Interrupt Response Manager

- 96 dedicated PIE vectors
- No software decision making required
- Direct access to RAM vectors
- Auto flags update
- Concurrent auto context save

Auto Context Save	
T	ST0
AH	AL
PH	PL
AR1 (L)	AR0 (L)
DP	ST1
DBSTAT	IER
PC(msw)	PC(lsw)

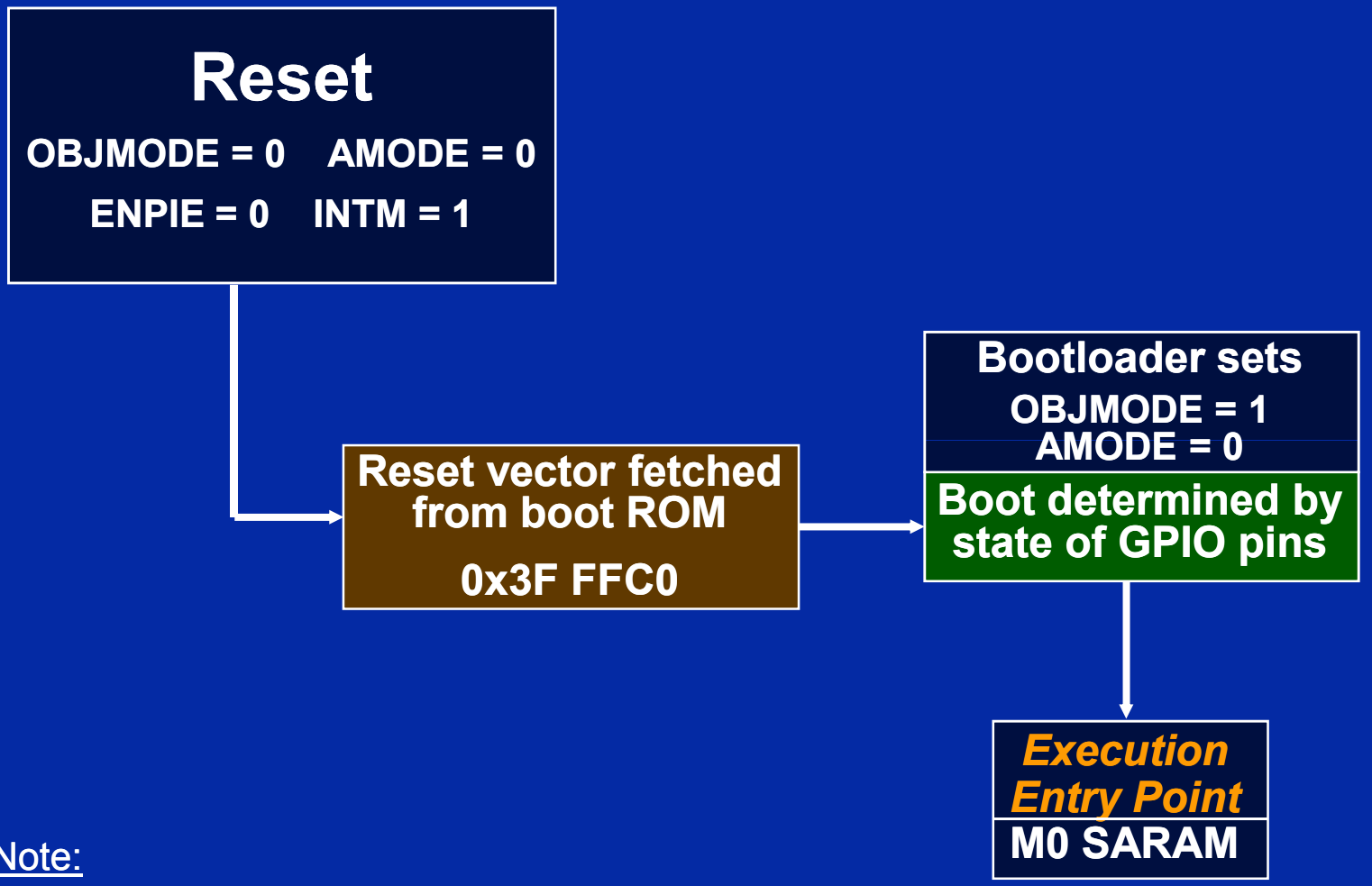


F2833x Operating Modes

Mode Type	Mode Bits OBJMODE	AMODE	Compiler Option
C28x Native Mode	1	0	-v28
C24x Compatible Mode	1	1	-v28 –m20
Test Mode (default)	0	0	
Reserved	0	1	

- Almost all uses will run in C28x Native Mode
- The bootloader will automatically select C28x Native Mode after reset
- C24x compatible mode is mostly for backwards compatibility with an older processor family

Reset – Bootloader



Note:

Details of the various boot options will be discussed in the Reset and Interrupts module

Highlights of the F2833x

- High performance 32-bit DSP
- 32x32 bit or dual 16x16 bit MAC
- IEEE single-precision floating point unit
- Atomic read-modify-write instructions
- Fast interrupt response manager
- 256Kw on-chip flash memory
- Code security module (CSM)
- Control peripherals
- 12-bit ADC module
- Up to 88 shared GPIO pins
- Watchdog timer
- DMA and external memory interface
- Communications peripherals