A Delay Locked Loop for Analog Signal

Goran Jovanović[1], Mile Stojčev[2]

Abstract – **In this paper, we have presented a phase loop for controlling a chain of g_m–C all–pass filters. It's called Delay Locked Loop for Analog Signal Processing, and it's used for signal's phase regulation. 0.35 μm CMOS technology was used for design and verification of the circuit. According to the obtained results, we have concluded that it is possible to obtain a phase regulation in a wide frequency range, from 100 kHz up to 100 MHz.**

Keywords – **All-pass filter, OTA, Continual g_m–C filter, Delay Locked Loop.**

I. Introduction

Correct timing is always imperative for proper operation of complex electronic systems composed of digital and analog circuits. The quality of excitation signals (clock pulses and carriers) is determined by several factors including stable frequency and phase, property duty-cycle, and small jitter and clock skew. A good design solution is one that minimizes the impact of all previously mentioned negative effects issues.

In addition, correct phase characteristic is necessary for proper operation of some high-performance analog and radio-frequency (RF) circuits. Traditionally, Phase Locked Loops (PLLs) are used for high-frequency clock and carrier synthesis. When frequency multiplication is not required, a Delay Locked Loops (DLLs) offer better performance in respect to PLLs, since its design is easier, and both immunity to on-chip noise and stability of operation is better.

Development of analog DLL circuits was in focus of interest of several researchers during the last decade. In References [3], [4], all-analog multiphase DLL architectures that achieve both wide range of operation and low jitter performance are described.

In this paper we present efficient hardware architecture of an analog DLL building block suitable for implementation in analog and RF circuits such as modulators, demodulators, frequency converters, etc. The proposal is used as constituent for analog signals phase correction.

This paper is organized as follows. Section 2. specifies realization of first order g_m–C all–pass filter. Section 3. describes the new proposal structure of delay locked loop for analog signal processing. Details that relate to realization of the all-pass filters, charge pump, low pass filter and dynamic phase detector are given in Section 3, too. HSpice simulation results of DLL for analog signal are presented in Section 4. Finally, the conclusion is given in Section 5.

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II. Voltage Controlled All Pass Filters

Without influence on signal amplitude, the phase of an analog signal can be varied with all-pass filter. Within DLL we will use an all-pass filter as a circuit for phase adjustment. The main reason for such design solution is its suitability for implementation in VLSI IC CMOS technology.

The scheme of a first-order all-pass filter is given in Fig. 1(a). After substituting the Operational Transconductance Amplifier (OTA) with a transconductance g_m we obtain an equivalent electrical model presented in Fig. 1(b).

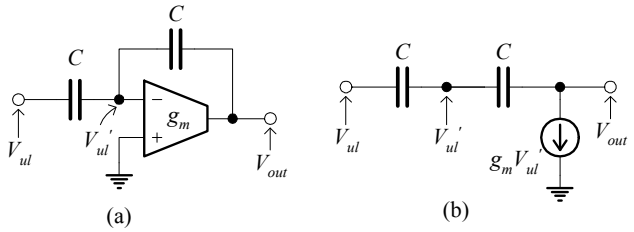

Fig. 1. (a) Scheme of the all-pass filter, (b) electrical model

The all-pass filter can be realized as a continuous g_m–C filter [6]. OTA and capacitors are used as filter's building blocks. For the circuit sketched in Fig. 1(b), we obtain the following transfer function

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{s - \frac{g_m}{C}}{s + \frac{g_m}{C}}. \quad (1)$$

According to Eq. (1) we have

$$\left| H(j\omega) \right| = 1, \quad (2)$$

and the phase characteristics is given as

$$\theta(s) = -2\arctan\left(\frac{\omega C}{g_m}\right). \quad (3)$$

The characteristic given by Eq. (3) is defined in term of admittance ωC and amplifier's transconductance g_m. Here, at disposal we have two design choices. Namely, the phase can be adjustment both by varying C or g_m. From aspect of CMOS technology, better and efficient solution, is one based on controlling the transconductance g_m, what is our design decision.

The scheme of OTA implemented in the all-pass filter is pictured in Fig. 2. It is a standard solution composed of: i) differential input stage (transistors M_1, M_2 and M_3); ii) three current mirrors (M_4, M_6; M_5, M_7; M_{10}, M_{11}, M_{12}, M_{13}) and; iii) an asymmetrical output (M_9, M_{11}). The OTA was

implemented in 0.35 μm CMOS technology, with supply voltage V_{dd} =3.3 V. As a result we obtained circuit with open loop gain A_0 = 80dB, first pole on f_p = 400 kHz, and an output resistance R_{out} = 6 MΩ.

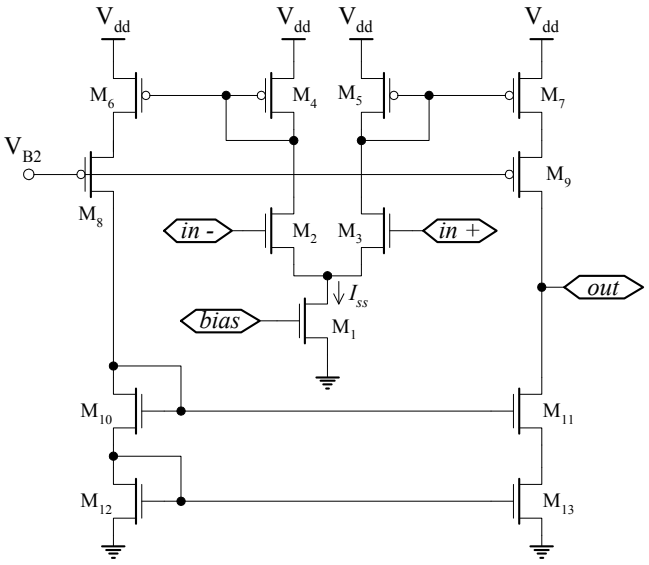

Fig. 2. Scheme of OTA

Let note that the polarization of transistor M_1 is non-standard. Namely, directly the gate of M_1 is connected to a bias control voltage V_{bias}, which represents output control voltage of the DLL loop filter (in essence V_{bias} corresponds to V_{ctrl} in Fig. 4). This voltage V_{bias} defines the sink current of a differential stage (transistors M_2, M_3) I_{SS}. The transconductance of the differential stage, g_{md}, is given by

$$g_{md} = \sqrt{\mu C_{ox}\left(\frac{W}{L}\right)_{M_2,M_3} I_{ss}} \qquad (4)$$

where I_{SS} is

$$I_{ss} = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_{M_1}\left(V_{bias} - V_{Th}\right)^2 . \qquad (5)$$

For more details related to Eq. (4) and (5) see Reference [1]. Implementing OTA with as voltage controlled transconductance on obtain voltage controlled *gm–C* all-pass filter [5]. HSpice simulation witch relates to phase transfer function of a first-order all-pass filter (Fig. 1), where OTA from Fig. 2 was used with capacitor C = 10 pF, is presented in Fig. 3. Simulations were carried in the frequency range from 1 kHz up to 1 GHz, for different values of control voltage V_{bias}, from 0.4 up to 0.9 V. By analyzing obtained results, we can conclude the following: i) the phase shift, for all transfer functions, starts from 180° (lower limit) and ends with 360° (upper limit); ii) by changing V_{bias} from 0.4 to 0.9 V the mid point (phase degree of 270°) shifts towards higher frequencies. For example, for V_{bias} = 0.4 V, phase shift 270° the frequency is 100 kHz, while for V_{bias} = 0.9 V, phase shift 270° the frequency is 100 MHz, what corresponds to the phase shift of three order quantities.

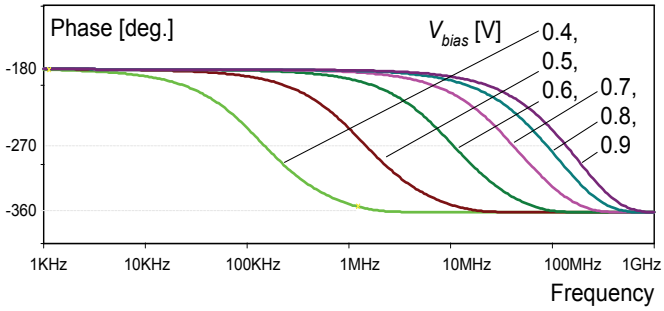

Fig. 3. Phase transfer function of *gm–C* all-pass filter related to frequency and V_{bias} voltage

III. Delay Locked Loop for Analog Signal Processing

When several voltage–controlled g_m–C filters are connected in a chain, then the ratio V_{out} / V_{in} is constant, while the phase of the V_{out} can be adjusted in a wide range. A phase-loop is used for controlling the chain of all-pass filter. The basic idea of phase controlling is similar to one which we meet in DLL circuits, with one exception: Instead to control pulse delay such as in digital DLL circuits, in this case we control the phase. The block diagram of the proposed circuits is given in Fig. 4.

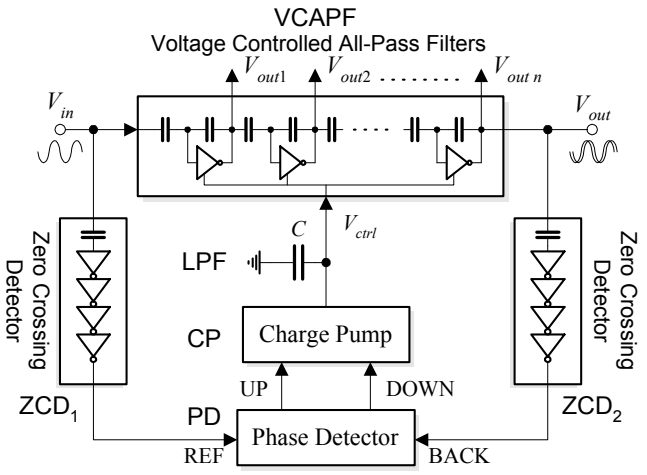

Fig. 4. Block scheme of DLL for analog signals

In order to evaluate a phase shift between V_{out} and V_{in}, it is first necessary to amplify these signals and after that to shape these signals to rectangular. This activity is achieved by using a zero crossing detector (ZCD). Phase comparison is achieved by a phase detector, PD. At its outputs the signals UP and DOWN are generated. The signal DOWN signal is active when V_{out} is leads (time advanced) in respect to V_{in}. In contrary the signal UP is generated. Time duration of UP and DOWN signal is proportional to the phase shift. Charge pump (CP) operation is controlled by UP and DOWN signals. The CP charges and discharges load capacitor C. V_{ctrl} is used as control voltage of a voltage controlled all–pass filter (VCAPF). When the DLL for analog signals is correctly locked the phase difference between V_{out} and V_{in} is 360°.

A. Chain of Voltage Controlled All–pass Filters

The phase transfer function of *n*-taps all-pass filter is defined by

$$\theta_n(s) = -2 \cdot n \cdot \arctan\left(\frac{\omega C}{g_m}\right) \qquad (6).$$

where *n* correspond to the number of taps in a filter. Phase shift at the output of each tap is given by

$$\theta_i(s) = -2 \cdot i \cdot \arctan\left(\frac{\omega C}{g_m}\right), \qquad 1 \le i \le n \qquad (7).$$

This means that at the output of a chained all–pass filter multi-phase signals, $V_{out\,1}$, ...,$V_{out\,n}$ are generated. In our case a chain of four taps was used.

B. Zero Crossing Detectors

The circuit by which we implemented ZCD is pictured in Fig. 5. It is composed of four inverter stages, A_1 to A_4. The first stage, A_1, acts as a linear amplifier. It is capacitive coupled both with the input and the output of a VCAPF. The other three stages, A_2, A_3 and A_4, are realized as (digital) inverter stages.

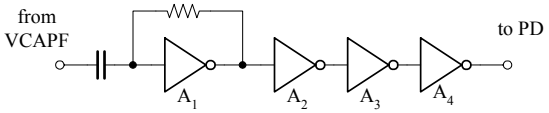

Fig. 5. Zero crossing detector

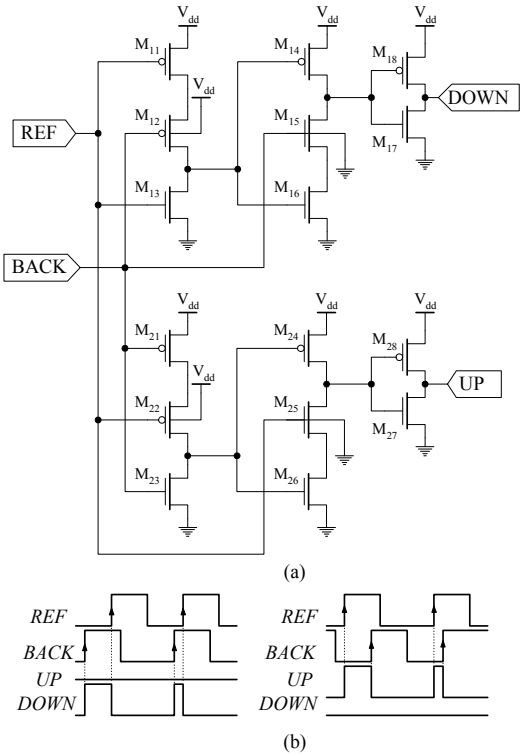

Fig.6. (a) Scheme of dynamic phase detector, (b) signals waveforms

C. Phase Detector

The phase detector (PD), given in Fig. 6(a), senses a phase difference between the reference signal, REF (output of ZCD_1), and the signal BACK (output of ZCD_2). Its hardware structure is adopted from Reference [2]. The main advantages of PD are: i) simple hardware structure; ii) high-speed of operation; and iii) small dead zone [2], [3]. PD's output signals, UP and DOWN, are used to control the operation of a charge-pump circuit, CP. The PD is sensitive to rising pulse edges.

Principles of PD's operation are presented in Fig. 6(b). The width of UP and DOWN signals is proportional to the phase difference between REF and BACK signals. Waveforms on the left side of Fig. 6(b) correspond to a case when the signal BACK leads in respect to the signal REF. Timing diagrams on the right side are valid when REF leads the BACK pulse.

D. Charge Pump and Low–pass Loop Filter

The charge-pump and loop filter structure are presented in Fig. 7. Transistors P_1 and N_1 act as switching elements driven by pulses UP and DOWN, while transistors P_2 and N_2 are employed as current sink and source, respectively. The charge-pump charges or discharges the filter capacitor, *C*. The voltage V_{ctrl} define VCAPF's phase characteristic. The charge-pump implements a transfer function of an integrator.

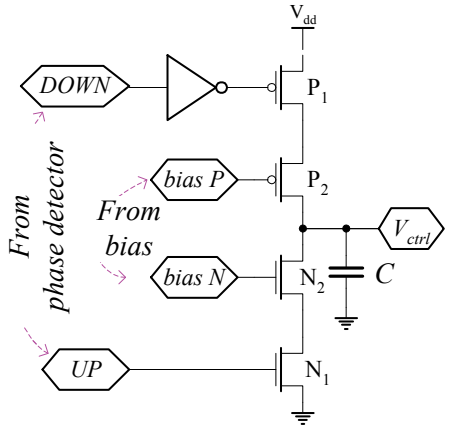

Fig. 7. Charge pump with loop filter

The capacitor, *C*, is used, as constituent of, the low-pass loop filter (LPF). Both, CP's current level, and charge delivered/accepted at every rising edge are set to small values [3]. This possibility allows easy implementation of the loop capacitor directly on a chip.

The bias circuit is intended to provide correct operation of CP. This block generates two control voltages, V_{bias_P} and V_{bias_N}. More design details concerning the bias circuit are given in Reference [7]. Control voltages, V_{bias_P} and V_{bias_N}, define the charge and discharge currents of a loop capacitor, *C*. Source and sink currents of P_2 and N_2, respectively, are equal and adjusted to be I_{CP} = 100 μA. The capacity of a low-pass filter *C* is 10pF.

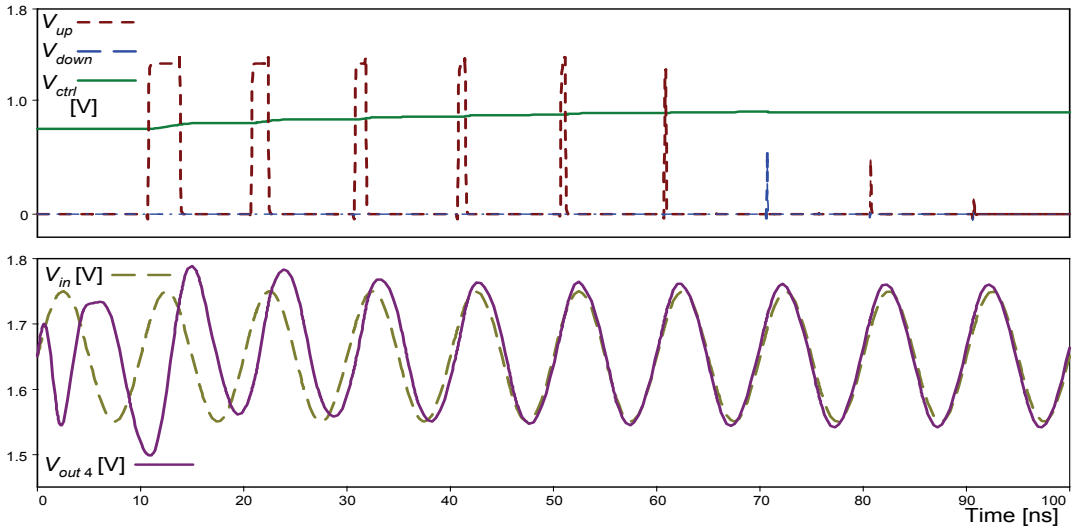

Fig. 8. DLL for analog signal transient simulation waveform

IV. Simulation

The design of a DLL for analog signals was verified using HSpice simulation. Models of level 47 that correspond to 0.35 μm CMOS technology were used. During simulation, the supply voltage V_{dd} was fixed to 3.3V, while the temperature T was held at 27°C.

Fig. 8, deals with HSpice simulation which relates to dynamics of establishing a stable state of the DLL circuit. In the lower part of Fig. 8, the input and output signals, V_{in} and V_{out4} respectively, for f = 100 MHz, are sketched. At the upper part, the waveforms obtained at the outputs of a phase detector, UP, DOWN, and V_{ctrl}, are given. The locking state is characterized at instant when: a) Full agreement between signals, V_{in} and V_{out}, exists; b) UP and DOWN signals disappear, and; c) a control voltage, V_{ctrl}, has a constant value. The elapsed time, from the start to the instant of establishing a stable locking state, is approximately 80 ns, and is satisfactory for numerous type of applications including modulators, demodulators, frequency converters, etc.

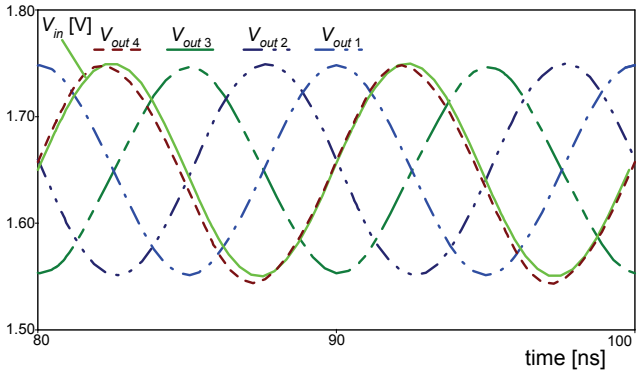

Fig. 9. Waveform of signals on outputs of all-pass filters

Fig. 9 presents waveforms of signals obtained on the outputs of four tap all-pass filter (VCAPF) when DLL is in a steady-state. As can be seen from Fig. 9, the phase shift between input and output signals, V_{in} and $V_{out\,4}$, is 360°. Also, the phase shift between adjacent taps of the filter's chain is 90°.

V. Conclusion

A DLL circuits intended for analog phase shift control is presented in this paper. Special care was devoted to realization of a chain of all-pass filters as constituent of a DLL circuit. The phase shift of a filter sections is controlled by a voltage obtained at the output of a phase–loop. Filter taps in VLSI CMOS are implemented as continual g_m–C filters.

The proposal has four taps and can be used for generating signals in quadrature. The DLL for analog signal is suitable for implementation of different types of modulators and demodulators, suppressing symmetrical signals in up/down frequency converters, etc. According to the obtained results, it is possible to obtain a phase regulation in a wide frequency range, from 100 kHz up to 100 MHz.

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