An Adaptive Pulse-Width Control Loop

G. Jovanović, D. Mitić, and M. Stojčev

Abstract - In high-speed CMOS clock buffer design, the duty cycle of a clock is liable to be changed when the clock passes through a multistage buffer [1]. In this paper, we propose a pulsewidth control loop referred as APWCL (Adaptive Pulsewidth Control Loop) that adopts the same architecture as the conventional PWCL, but with two modifications. The first one relates to implementation of the pseudo inverter control stage (PICS), while the second to involvement of adaptive control loop. The first modification provides generation of output pulses during all APWCL's modes of operation and the second faster locking time. For 1.2 μm CMOS process with V_{dd}=5V and operating frequency of 100MHz, results of SPICE simulation show that the duty cycle can be well controlled in the range from 20% up to 80% if the loop parameters are properly chosen.

I. Introduction

In high-speed design, a multistage clock buffer implemented into a long inverters chain is often needed to drive a heavy capacitive load. It is difficult to keep the clock duty cycle at 50% for these design solutions. When the clock signal passes through a multistage buffer, the symmetrical pulse-width may be destroyed due to the unbalance of the N and P channel transistors in the long buffer. This unbalance is introduced by many factors, such as process deviations, temperature changes, or mismatch in design. Consequently, the clock duty cycle will wonder away from 50%. In the worst case, as the pulsewidth becomes too narrow or too wide, the clock pulse may disappear inside the clock buffer [1], [5]-[8].

In systems that adopt a double data rate technology, both rising and falling edges of the clock are used to sample input data. These systems require the duty cycle of the clock to be precisely maintained at 50%. Therefore, an important issue is how to generate a clock with precise 50% duty cycle for high-speed operation [2]. Automatic control technology, such as pulsewidth control loop (PWCL) has been used for adjusting the output duty cycle of multistage driver for several years and was described by [1]- [4].

In this paper, architectural description and principle of operation for conventional types of PWCLs, already well known from literature, covered is in Section II. Section III, describes the structure of the proposal, referred as adaptive pulsewidth control loop. Details related to APWCL implementation and simulation results are given in Section IV. Section V gives a conclusion to this paper with summary.

G. Jovanović, D. Mitić, and M. Stojčev are with the Faculty of Electronic Engineering, University of Niš, Aleksandra Medvedeva 14, 18000 Niš, Serbia & Montenegro, E-mail: joga@elfak.ni.ac.yu

II. Conventional PWCL

Schematic diagram of the conventional PWCL [1] is pictured in Fig. 1. As it can be seen from Fig. 1, the conventional PWCL is realized as a system with feedback loop.

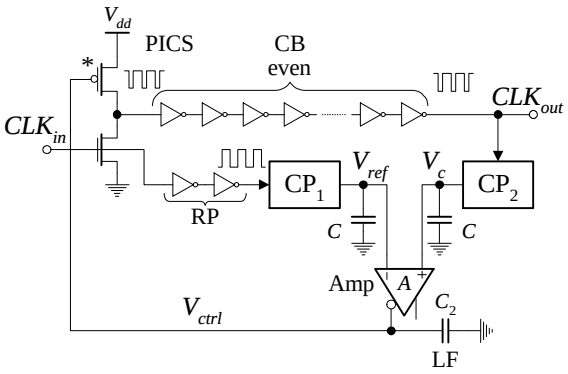

Fig. 1. Conventional PWCL

The feedback loop functionally consists of:

(a) Pseudo-Inverter Control Stage (PICS) - chosen to be the first stage of the clock buffer and functions as a voltage-controlled pulse-generator. By changing the control voltage, V_{ctrl}, we can adjust the pulsewidth of the output clock. PICS is implemented as a simple inverter. Mark "*" indicates the controlled transistor;

(b) Clock Buffer (CB) - a long inverter chain or buffer which acts as a multistage driver;

(c) Charge Pump 1 (CP1) - converts pulsewidth into current which charges or discharges capacitor C. At its output, CP1 creates a reference voltage V_{ref}, by connecting to a reference clock with 50% duty cycle;

(d) Charge Pump 2 (CP2) - is another identical charge pump that creates a voltage V_c, i.e. it steers current by the clock pulse CLK_{out} for detecting the change of pulsewidth;

(e) Amplifier (Amp) - the amplifier is characterized by its gain *A*, realized as a differential amplifier. It is intended to provide a certain gain in the loop at low frequency;

(f) Reference Pulse (RP) - two stage inverter buffers used to drive CP1 with 50% duty cycle referent clock pulses;

(g) Loop Filter (LF) - the output resistor of Amp and capacitor C_2 form a first-order low-pass filter.

In Fig. 1 two identical single-ended charge-pumps are used. One of them is used for detecting the pulsewidth of the clock being controlled, and another is connected to a standard clock with 50% duty cycle for generating V_{ref}. The voltage V_{ref} is taken as reference voltage. The charge-

pumps, CP1 and CP2, and the differential amplifier, Amp, are constituents of the duty cycle comparator. The output voltage V_{ctrl} controls the operation of PICS.

The pulsewidth of CB is controllable. This means that if the CB's clock output deviates from 50% duty cycle, the control voltage, V_{ctrl}, will change so that the offset can be removed. When the loop is stable the CB output is adjusted to 50% duty cycle, and the controllable dynamic range covers the range of possible offset.

III. ADAPTIVE PWCL

Block diagram of the APWCL is sketched in Fig. 2. From functional point of view, the following building blocks can be identified:

(a) Pseudo-Inverter Control Stage (PICS) – at the output, $PICS_{out}$, pulses of variable duty cycle are generated. V_{ctrl}, is used as an input control voltage;
(b) Clock Buffer (CB) – an inverter chain implemented as odd (even) stages clock driver;
(c) Charge Pumps (CP*x*) – two voltage controlled charge pump circuits, CP1 and CP2, of different structure;
(d) Reference Pulse (RP) – chain composed of two inverters;
(e) Bias Circuits (BC1 and BC2) – provide control voltages for transistors polarization of CP1, CP2 and PICS;
(f) Differential-input differential-output operational amplifier (Amp) – acts as an inverting (non-inverting) amplifier in a feedback control loop. For odd (even) number of stages in CB the Amp is implemented as non-inverting (inverting) amplifier;
(g) Low-pass filter (LF) – filter element in a feedback control loop;
(h) Charge Pump Controller (CPC) – is implemented as differential amplifier. At its output, the CPC generates control voltage V_A that is proportional to $V_{ref} - V_c$ on voltage difference.

In respect to the conventional PWCL proposed by Fenghao and Svensson [1], there are several novelties involved into APWCL. The first one relates to the PICS, while the second to CP2. In addition, two new building blocks, CPC and BC2 are included into APWCL structure. The other constituents, pictured in Fig. 2, are of identical (or almost-identical) architectures as those described by [1].

The signals CLK_{in} and CLK_{out} are input and output pulse signals of APWCL, respectively. They drive two charge pumps, denoted as CP1 and CP2 (Fig. 2). The output voltage V_{ref} (V_c) of the charge pump CP1 (CP2) is directly proportional to the duty cycle of the input signal CLK_{in} (CLK_{out}). Charge pump CP1 (CP2) load capacitor C_{11} (C_{12}) is discharged during the positive pulse period and charged in the rest of the period. The charging and discharging currents are adjusted to be identical. The signal CLK_{in} is selected as a referent one. Its duty cycle is 50%. Therefore, the voltage V_{ref} at the output of CP1 is referent.

Due to influence of different propagation delays of the leading and trailing edges of the clock signal, when it passes through the long chain clock buffer, the duty cycle of the CLK_{out} become unsymmetrical, i.e. different from 50%.

The voltages V_{ref} and V_c drive the differential amplifier (Amp). Voltage V_{ctrl} is generated at the Amp's output. The V_{ctrl} controls operation of the PICS. When the APWCL is in steady-state, the magnitude of control voltage V_{ctrl} causes the duty cycle of the CLK_{out} to be 50%.

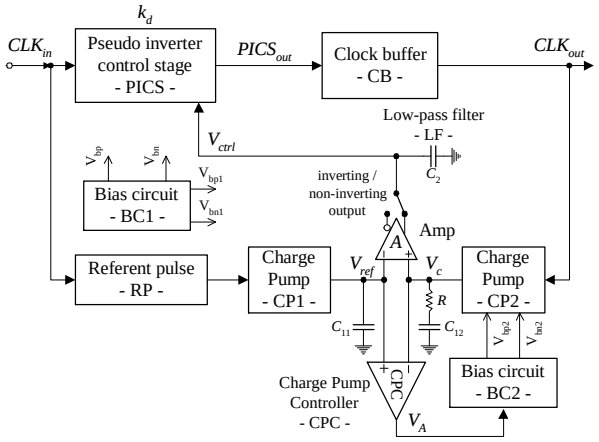

Fig. 2. Block diagram of APWCL.

A. *Pseudo Inverter Control Stage - PICS*

An electrical scheme of the PICS is pictured in Fig. 3(a). It consists of three N-channel N_1, N_2 and N_3, and three P-channel P_1, P_2 and P_3, transistors. The PICS's equivalent electrical scheme is presented in Fig. 3(b). Transistors P_1 and P_2 act as constant and variable current sources J_1 and J_2, while transistors N_1 and N_2 operate as constant and variable current sinks I_1 and I_2, respectively. Transistors P_3 and N_3 belong to the switching parts of the CMOS inverter. Capacitor C_L represents a parasitic capacitive load.

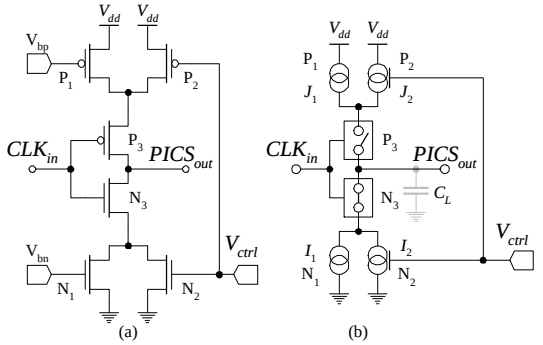

Fig. 3. The block PICS: (a) electrical scheme, (b) equivalent scheme.

The amount of the current of the constant current source (sink) J_1 (I_1) indirectly determines the nominal time delay of the leading (trailing) pulse edge at the output $PICS_{out}$. The bias voltage V_{bp} (V_{bn}) is used for polarization

of transistor P_1 (N_1). The variable current source (sink) J_2 (I_2) indirectly defines the variable time delay of the leading (trailing) pulse edge. Such a configuration, allows us to achieve controllable time delay for both, leading and trailing pulse edges.

In Fig. 4, the range of duty cycle variation, in terms of V_{ctrl}, is shown. Again, duty cycle of 50% for $V_{ctrl}=V_{dd}/2=2.5$V is achieved. When V_{ctrl} decreases the duty cycle increases, by contraries it decreases.

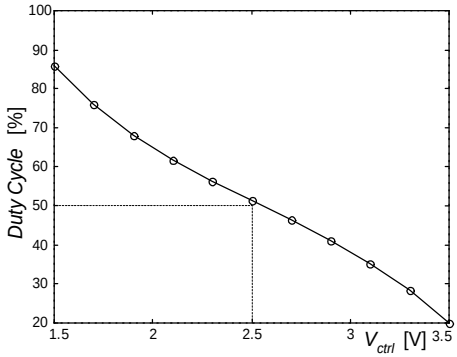

Fig. 4. Duty cycle in term of V_{ctrl}.

B. *Parallel charge pump - CP2*

The charge pump CP2, pictured in Fig. 5, is composed of two charge pumps, $CP2_1$ and $CP2_2$, that operate in parallel. The structure of the pump $CP2_1$ is identical with CP1. The bias circuit BC2 provides polarization for $CP2_2$. The block CPC (Fig. 2) defines the magnitude of the control voltage V_A.

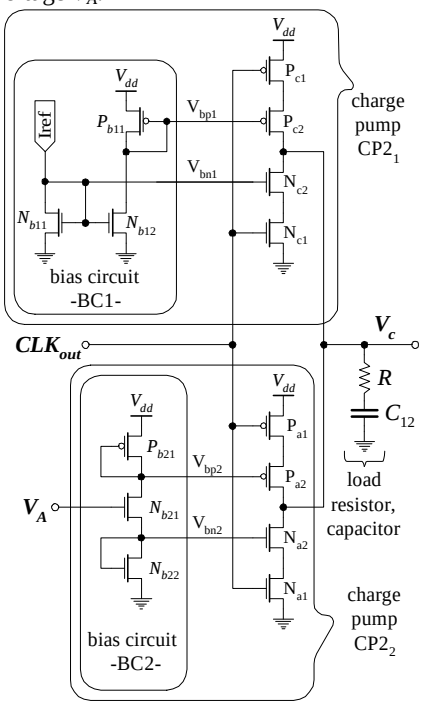

Fig. 5. Electrical scheme of CP2 charge pump.

The load impedance of CP2 is realized as a serial connection of resistor R and capacitor C_{12}. This connection involves one zero in the transfer function of CP2, and also in a transfer function of the APWCL. Involving zero in the APWCL's transfer function allows us to adjust the damping factor x to optimal value (x=0.707), and to decrease the transition time in the linear mode during the period of establishment of a steady-state.

IV. APWCL SIMULATION RESULTS

SPICE simulation results for APWCL circuit in a 1.2μm CMOS process with V_{dd}=5V supply voltage and operating frequency 100MHz, are presented in Fig. 6. Comparative, results that relate to the conventional PWCL and proposed APWCL, in Fig. 6(a) and (b), are given respectively. Identical building blocks PICS, CP1, Amp, BC1 are used for both simulations. In both cases, the clock buffer (CB) has 7 stages with tapering factor of 1. Related to conventional PWCL, CP2 is replaced with charge pump whose current is variable in APWCL charge pump. Additional blocks CPC and BC2 are used for current regulation in charge pump CP2.

The circuit's model in linear mode is described by the second order transfer function [2]. The desire system's dynamic is defined by choice of the dumping factor x and natural frequency w_n. The dumping factor is x=0.707 and natural frequency is $w_n=3\cdot10^7$ rad·s^{-1}. Other circuits parameters are determined as: $I_{cp1}=I_{cp2}=I_{cp}$=10μA – corresponds to charge pump current of CP1 and $CP2_1$; A=100 – DC gain of the Amp; $w_0=2\pi f_0=2\pi$ 3.5MHz – dominant pole of the Amp; $C_{11}=C_{12}=C$=8pF – charge pump capacitor; R=2800Ω – CP2 load resistance; k_d=0.32V^{-1} – PICS's sensitivity constant. For nonlinear operating mode $I_{cp2}= I_{cp}+I_{cp}$' where I_{cp}'=50μA.

The waveforms at the top in Fig. 6(a) and (b) correspond to curves of V_{ref} and V_c. The second waveform in Fig. 6(a) corresponds to the control voltage V_{ctrl}. Additionally, in Fig. 6(b), the control voltage V_A, is presented. The two lower waveforms in Fig. 6(a) and (b), depict CLK_{out} pulses valid for nonlinear mode and steady-state mode, respectively.

We start with our simulation from the instant when the system is powered-on ($t=t_0$). This implies that both charge pumps load capacitors, C_{11} and C_{12}, as well as the low-pass filter capacitor C_2, are discharged. According to the transient response, the following three different modes, in the operation of the feedback loop, can be identified:

a) From t_0 up to t_1 the loop operates in nonlinear mode. Since C_{11} charges faster, in respect to C_{12}, at instant t_0 the voltage V_{ref} becomes greater than V_c and therefore the output of Amp switches rapidly to lower voltage limit, and the control voltage V_{ctrl} is 0V. Under this condition at the CLK_{out}, pulses of minimal pulsewidth are generated. Contrary to the proposals described by [1] and [2], where in the saturation mode the PWCL is inoperative, i.e. CLK_{out}

is blocked, in APWCL pulses of minimal duty cycle, at the output of CLK_{out}, are generated.

b) As the input voltage difference becomes small enough, the amplifier Amp enters linear mode what corresponds to the time interval from t_1 up to t_2. When the dumping factor ξ=0.707, transients in linear mode are minimal.

c) Steady-state operation mode characterizes stable-loop operation and corresponds to the time interval after t_2. During this period, variations of V_{ctrl} are less than ±25mV, i.e. 1.8% in respect to V_{ctrl} (1.5V). As it can be seen from Fig. 6, the duty cycle of CLK_{out} in the saturation mode is 20%, and in the steady-state mode it is 51%.

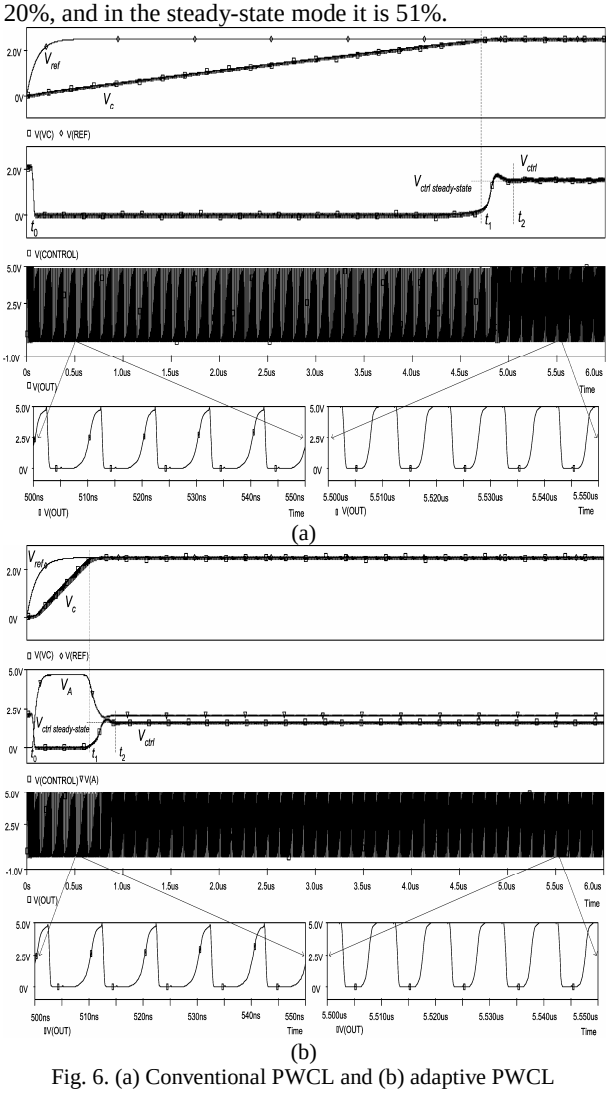

Fig. 6. (a) Conventional PWCL and (b) adaptive PWCL simulation results.

The main difference between waveforms in Fig. 6 (a) and waveforms in Fig. 6(b) relates to the time duration of nonlinear operating mode, from t_0 up to t_1. The voltage difference between V_{ref} and V_c during this period is large and the differential amplifier CPC enters in saturation region. The CP2's control voltage V_A is approximately equal to the supply voltage V_{dd} and the current I_{cp}' is active. This means that in nonlinear mode the charge pump CP2 works with current $I_{cp2}=I_{cp}+I_{cp}'=n\ I_{cp}$=60μA. Increasing CP2's current by a factor n means that the time duration of nonlinear mode t_{NL} is shortened by n, too. This possibility provides a condition for fast loop locking time.

V. Conclusion

The clock distribution tree within the VLSI ICs is so large and carries so much capacitance that buffers need to be inserted just to be able to drive the clock-tree in order to have a reasonable clock waveform. When the clock passes through a multistage buffer changes its duty cycle. In order to obtain a satisfactory duty cycle correction a fast locking APWCL was proposed. The APWCL adopts almost identical architecture as conventional PWCL [1]-[3] but with two modifications. The first relates to implementation of the pseudo inverter control stage (PICS), which is operative during all APWCL's mode of operation. This possibility provides pulses generation at the output of APWCL during all mode of operation. The second modification represents involvement of adaptive control loop, which provides shorter transient time of the nonlinear mode, i.e. faster locking time. SPICE simulation results, for 1.2μm CMOS process with V_{dd}=5V and 100MHz operating frequency, show that the duty cycle can be controlled in the range from 20% up to 80%.

References

[1] M. Fenghao, C. Svensson, "Pulsewidth Control Loop in High-Speed CMOS Clock Buffers, " *IEEE Journal of Solid-State Circuits*, vol. 35, No. 2, pp. 134-141, February 2000.

[2] H. Sung-Rung, L. Shen-Iuan, "A 500-MHz–1.25-GHz Fast-Locking Pulsewidth Control Loop With Presettable Duty Cycle," *IEEE Journal of Solid-State Circuits*, vol. 39, No. 3, pp. 463-468, March 2004.

[3] Y. Po-Hui, W. Jinn-Shyan, "Low-Voltage Pulsewidth Control Loops for SOC Applications," *IEEE Journal of Solid-State Circuits*, vol. 37, No. 10, pp. 1348-1351, October 2002.

[4] M. Yongsam, C. Jongsang, L. Kyeongho, J. Deog-Kyoon, K. Min-Kyu, "An All-Analog Multiphase Delay-Locked Loop Using a Replica Delay Line for Wide-Range Operation and Low-Jitter Performance, " *IEEE Journal of Solid-State Circuits*, vol. 35, No. 3, pp. 377-384 , March 2000.

[5] M. Flynn, P. Hung, K. Rudd, "Deep–Submicron Microprocessor Design Issues," IEEE Micro, vol. 19, No. 4, pp. 11-22, 1999.

[6] J. Maneatis, F. Klass, C. Afghani, *Timing and Clocking*, pp. 10.1-10.34, in The Computer Engineering Handbook, ed. by Oklobdzija V., CRC Press, Boca Raton, 2002.

[7] V. Oklobdzija, M. Stojanović, M. Marković, N. Nedović, *Digital System Clocking: High-Performance and Low-Power Aspects*, Wiley Interscience, New York, 2003.

[8] J. Öberg, *Clocking strategies for Networks-on Chip, in Networks on Chip*, eds. by Jantsch A., and Tenhunen H., Kluwer Academic Publishers, Boston, 2003.