Power Reduction Technique for Successive-Approximation Analog-to-Digital Converters

Dragan B. Stankovic[1], Mile K. Stojcev[1], Goran Lj. Djordjevic[1]

***Abstract* – This paper addresses the problem of reducing power consumption in successive approximation ADC architecture as a building block of power-aware electronic devices. Two binary search control algorithms, intended to decrease the total ADC's consumed energy during the conversion cycle are proposed in this paper. Both algorithms take advantage of sensor input signal properties and dynamically reduce the number of conversion steps in order to save energy. Metrics for evaluating energy efficiency of the conversion process, called energy reduction factor, F_{er}, is involved. Simulation results show that energy saving per conversion cycle of up to 25 % can be obtained.**

***Keywords* – Low power, ADC, SAR A/D converter**

I. INTRODUCTION

During the past period, much of the research on Analog to Digital Converters (ADCs) has been focused on development of new architectures (such as pipeline converters, folding converters, sub-ranging converters, and sigma-delta converters), that characterize an increasing sampling rate and resolution [1, 2, 3, 4]. While there are numerous applications (e.g. multimedia, communications) that demand such advances, other engineering applications (e.g. biomedical, wireless sensor networks) do not require high performance but focus on portion of the ADC design space that has received comparatively little attention - moderate resolution and speed, but ultra-low power [5, 6].

In this paper we present an algorithm based approach for efficient reduction of ADC's power consumption. The proposal is implemented on a Successive Approximation Register - ADC (SAR-ADC), as a constituent of a power-aware device. The energy requirements for analog-to-digital conversion are explored and a system level optimization of energy per converted cycle of a SAR-ADC is performed.

II. ANALOG-TO-DIGITAL CONVERTER ARCHITECTURE

Used as the interface between the analog and digital portion, ADC is one of the key functional block of any mixed signal circuit and therefore must be optimally designed concerning both performance and power.

[1] Dragan Stankovic, Mile Stojacev and Goran Djordjević are with the Faculty of Electronic Engineering, Aleksandra Medvedeva 14, 18000 Nis, Serbia, E-mail: {gagi, stojcev, gdjordj}@elfak.ni.ac.yu.

In general, ADC architectures can be classified according to several equal criteria such as speed, resolution, power consumption, etc. For us more interesting is the classification scheme that is based on energy consumption which ADCs require for a single conversion cycle. For a 10-bit conversion several different architectures are compared in Table I.

TABLE I
COMPARISON OF ADC ARCHITECTURES

Architecture	Clock Cycles	# Amps	# Comp.	# Operations
Flash	1	0	1024	1024
Serial or Ramp	1024	1	1	2048
Algorithmic	10	1	2	30
SAR Charge Balancing	10	0	1	10
Sigma Delta	64	2	1	192
Pipelined	1	10	20	30

The results presented in Table 1 illustrate that the analog-to-digital technique based on SAR is the most energy efficient one, and can provide the lowest hardware cost.

The general architecture of the SAR-ADC is composed of four major parts. These are: a S/H circuit, a DAC, a Comparator, and a Successive Approximation Register and Control (see Fig. 1). Let note that in standard solutions the function of S/H circuit is realized by capacitor array of the DAC.

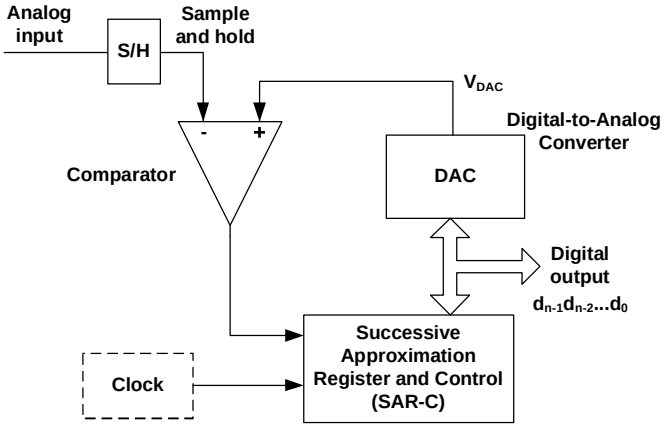


Fig. 1. Successive approximation analog-to-digital converter.

This ADC functions by iterating through values, via the SAR, until the DAC generated reference voltage, V_{DAC} , and the sampled analog input, Vn, are equal. Energy efficient operation is achieved thanks to the following facts:

- The final digital output code is available after the n^{th} comparison for *n*-bits resolution.

- This architecture is realized with minimal amount of analog hardware.
- In SAR-ADC the conversion time is relatively short (*n*-clock cycles), while the amount of installed analog hardware is minimal.
- Assuming that the digital logic contributes very little power to the total dissipation, we conclude that energy consumption is dominated by three processes:
  - charging the S/H capacitor;
  - charging the binary weighted capacitors, that are constituent of DAC, to reference voltage; and
  - *m* comparison operations, where *m* is the number of conversion steps, $1 \leq m \leq n$, in a case when conversion with reduced bits resolution is used.

It should be noted that any search algorithm, including reduced output resolution (case when $m \leq n$), could be implemented in the successive approximation architecture with the appropriate SAR_C logic. This makes the SAR-ADC architecture flexible for power-aware applications, since the search algorithm can be modified both to take advantage of input signal properties and to reduce dynamically the resolution during the conversion process.

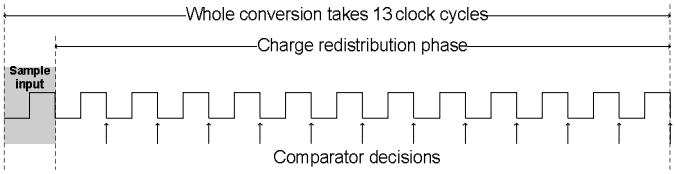
In order to achieve low power consumption we have decided to choose charge redistribution SAR-ADC as our design solution.

Let now analyze operation of the *n*-bit SAR-ADC in the following two modes of operation:

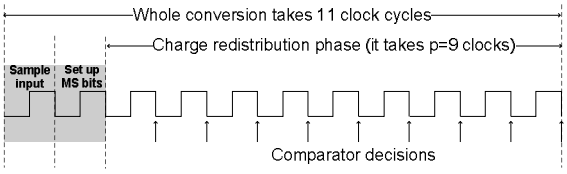
- Full conversion – typical for a classical *n*-bit conversion cycle [7, 8, 9].
- Reduced conversion – involved and defined in our proposal.

Waveforms that correspond to operation of 12-bit SAR-ADC in full- and reduced- conversion cycle are sketched in Fig. 2(a) and (b), respectively.

For completion of full conversion time interval of $(n + 1)$ clock cycles are needed.



(a) full conversion



(b) reduced conversion

Fig. 2. Timing diagram of SAR-ADC.

For reduced conversion one clock cycle for sampling is used, one clock cycle for setting-up the coincident MS bits is involved, and during the rest $(n - m)$ clock cycles charge redistribution phase is performed.

Assuming that the power consumption of the SAR-ADC, P_{ADC}, is constant during conversion cycle, the energies of SAR-ADCs with full (*n*-bit) and reduced (*p*-bit) conversion can be expressed by eq. (1), and eq.(2), respectively.

$$E(n) = (n+1)P_{ADC}t_{clk} \tag{1}$$

$$E(p) = (p+2)P_{ADC}t_{clk} \tag{2}$$

Now let form a metrics called energy-reduction factor, F_{er}, as a ratio between the $E(n)$-$E(p)$ and $E(n)$, i.e.:

$$F_{er} = \frac{E(n)-E(p)}{E(n)} \times 100[\%] = \frac{n-p-1}{n+1} \times 100[\%] \tag{3}$$

In the worst case, $p = n - 1$, we obtain $F_{er} = 0$, what means that there is no energy reduction, while for p = 0, we obtain:

$$F_{er} = \frac{n-1}{n+1} \times 100[\%] \tag{4}$$

Illustration only, for $n = 12$, the achievable energy reduction is within a range 0 – 84.6 %.

III. ALGORITHM DESCRIPTION

In this section, we present two power-saving SAR-ADC control algorithms that reduce the number of steps (clock cycles) needed to carry out a single conversion cycle. A fundamental assumption in our approach is that most of the time the difference between two successive samples is limited and much smaller then the full-scale, i.e. $|V_{a,k-1} - V_{a,k}| < \delta$, where $V_{a,k-1}$ is the previous and $V_{a,k}$ the next analog input signal value, and δ is the predicted maximal difference. Instead to perform a full conversion for each new sample, control algorithms use δ in order to identify the most significant bit sequence of the previous converted digital value that will stay unchanged and then perform conversion for the least significant bit sequence.

Algorithms differ in a way how the parameter δ (referred as a band size) is determined. For the first one, referred as Range Checking Algorithm (RCA), the band size is constant input parameter externally defined. For the second one, referred as Variable Range Algorithm (VRA), the band size is dynamically adjusted by the algorithm itself to accommodate the current signal dynamics.

The flow chart of the RCA algorithm, which defines the operation of SAR-ADC control logic during a single conversion cycle, is shown in Fig. 3. The inputs to the algorithm are the previous digital converted value, N_{k-1}, the digital equivalent of the band size, *d*, and the converter resolution, *n*. The algorithm generates the next digital value, N_k. At the beginning, the limits $N_{k-1} - d$ and $N_{k+1} + d$ of a measuring interval are calculated. Next, the number of most significant coincident bits, *m*, is determined. During this, a bitwise ExOR logical operation on lower, $N_{k-1} - d$, and higher, $N_{k+1} + d$, voltage-band limits is performed. The number of leading zero bits of the result is equal to *m*. After that, by calling the function *conv(m)*, *n-m* conversion steps are performed, starts from bit position *n-m*-1. Finally, a test

procedure, during which we check if the converted value lies within the expected interval $[N_{k-1} - d, N_{k+1} + d]$, is carried out.

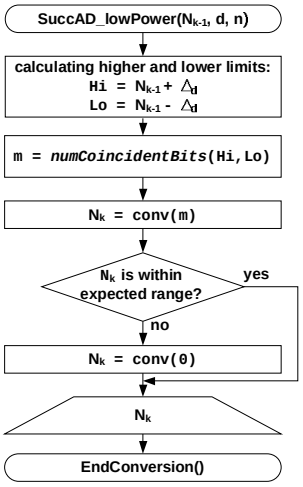


Fig. 3. SAR-ADC based on charge redistribution

The principle of operation of VRA can be described as follows. At the start of each conversion cycle, a difference between the last two samples is calculated and is used as *d* for the next conversion cycle. This means that during each conversion cycle the algorithm manipulates with different *d* value. As a consequence, if the dynamics of the input signal at some specific instant changes, then the difference between two successive samples (i.e. band) will change, too. So, a *d* increasing leads to band enlargement, while *d* decreasing to band compression.

IV. Simulation and Results

In order to evaluate the capabilities of the proposed algorithms a simulator, called ADC_sim, was developed.

We assume that our power-aware device acquires analog signals that characterize both high and low speed variations. These signals correspond to physical quantities such as:

- vibrations of acoustic or seismic energy detector which generates burst (shock) wave signals (typical for high speed signal variations); and
- low-speed signals generated at the output of the omni-directional sensors (typical examples for such sensors are thermometer, light sensors, smoke detector, pressure, etc.).

Independently of its nature and origin, the characteristics of each signal variation can be precisely analytically defined by some formula. In this way the power estimation of the SAR-ADC can be precisely modeled. In the sequel we will point to two typical input signal waveforms, periodical and burst.

Periodical input signal. Input signals with this property we approximate with the following equation:

$$x(t) = x_0 + x_1 \sin\frac{2p}{T}t + x_2 \sin(150\frac{2p}{T}t + j_k) + x_3 e(t) \qquad (5)$$

where: *x(t), y(t)* - sensed input signal; x_0 , y_0 – average analog input value (DC voltage); $x_1 \sin\frac{2p}{T}t$, $y_1 \sin\frac{2p}{T}t$ - slow speed component of the analog input signal with long period variation; $x_2 \sin(150wt + j_k)$ - medium speed analog input signal with short period variation; $x_3 e(t)$, $y_3 e(t)$ - noise (random variations of input signal).

Bursty input signal. This type of input signal (see Fig. 4) corresponds to seismic signal variations, and is defined by (6):

$$y(t) = \begin{cases} 0, & 0 \le t < 0.9T \\ A\sin w_1 t \sin w_2 t & 0.9T \le t < 0.9T + \frac{1}{4}T_1,\ T_1 = \frac{2p}{w_1} \\ A\sin w_2 t & 0.9T + \frac{1}{4}T_1 \le t < 0.9T + \frac{1}{2}T_1 \\ Ae^{-(t-0.9T+\frac{1}{2}T_1)} \sin w_2 t & 0.9T + \frac{1}{2}T_1 \le t < T \end{cases} \qquad (6)$$

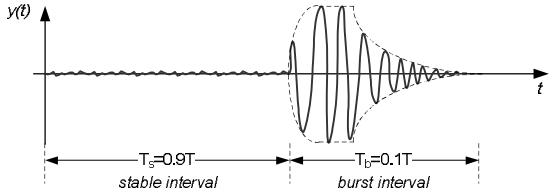


Fig. 4. Bursty signal.

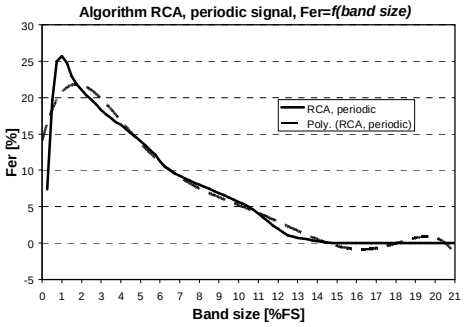
In order to evaluate ADC's performance during the simulation process we have used signal excitations defined in Subsection III.A. Parameters of input signals, for both input signals are defined in Table III.

TABLE III
PARAMETERS OF THE ANALOG INPUT SIGNALS

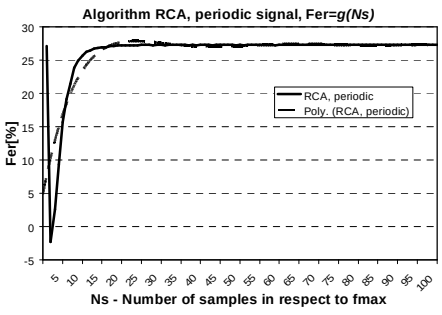
Type	**Parameters**
Periodic	x_0 =5.97, x_1 =0.43, x_2 = 0.17, x_3 =0.08, j_k = 0
Bursty	A=5.0, w_2=10w_1, T_{burst} = 0.1 T

Numerous simulations were performed. The number of samples per period was within the range of [300, 15000] for periodic, and [200, 10000] for bursty signals. The simulation results for both algorithms, RCA and VRA, are presented in Fig. 5 and 6. Figure 5 presents simulation results related to periodic input signal. Curves marked with full line correspond to real simulation results, while curves marked with dashed lines correspond to polynomial approximated results. In average, maximal value for F_{er} is 25 %. In Fig. 5(a) the maximum corresponds to a peak value, while in Fig. 5(b) and 5(c) the maximum is an asymptotic value. Optimal operating conditions (maximum F_{er}) for Fig. 5(a) correspond to the peak value (i.e. band size of 1% FS). For Fig. 5(b) and 5(c) optimal operating conditions represent the best compromise between F_{er} and N_s (the highest F_{er} for the smallest N_s) and correspond to the beginning of the saturation region (i.e. N_s = 12 for Fig. 5(b), and N_s=15 for Fig. 5(c)).

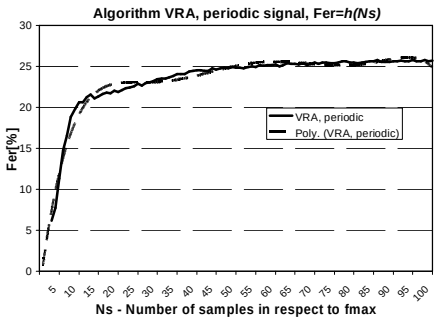
Simulation results that correspond to bursty input signal are presented in Fig. 6. By analyzing Fig. 6, we can conclude the following: The energy reduction factor F_{er} is comparable to periodic signal but it is relatively insensitive in respect to sampling frequency variations. Near-optimal band size for RCA is 4 % FS what as a consequence have F_{er} = *21* %. The energy reduction factor, F_{er}, for RCA is (20 – 23) %, and for VRA is (13-14) %.



(a) F_{er} achieved with RCA in terms of band size

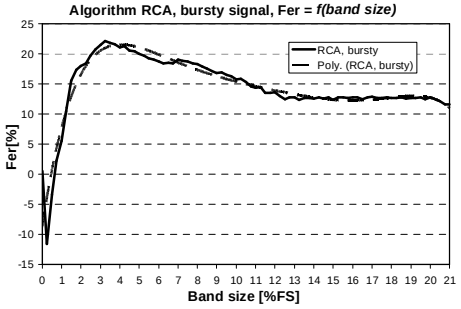


(b) F_{er} achieved with RCA algorithm in terms of sampling rate

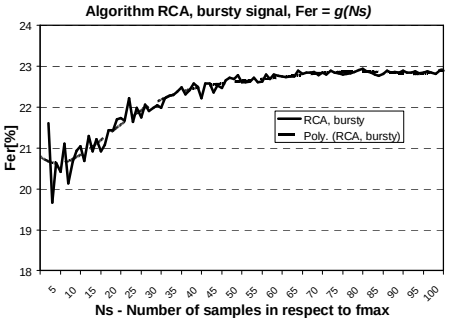


(c) F_{er} achieved with VRA in terms of sampling rate

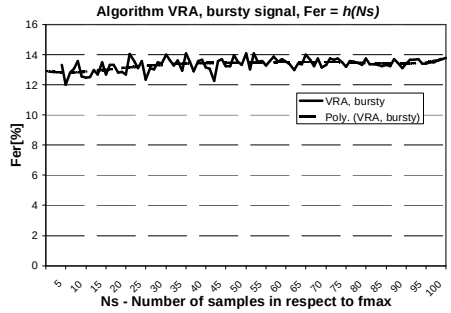
Fig. 5. Energy reduction factor (F_{er}) for periodic signal.



(a) F_{er} achieved with RCA in terms of band size



(b) F_{er} achieved with RCA algorithm in terms of sampling rate



(c) F_{er} achieved with VRA in terms of sampling rate

Fig. 6. Energy reduction factor (F_{er}) for bursty signal.

V. CONCLUSION

In focus of our interest was the problem of reducing power consumption that deals with the analog-to-digital conversion process. In order to evaluate the performance of the proposed algorithms we have involved a metrics called energy reduction factor. The obtained results implemented on a standard type of SAR-ADC show that high reduction percentage can be obtained if MS bits (typically 3 to 5) are correctly predicted.

In addition, we have proposed two algorithms for reducing energy consumption in SAR-ADC using predictive methods. Namely, we expect that the current sample will be located within the boundaries of a fixed or adaptive band-size in the vicinity of the previous sample. In order to evaluate the performance of the proposed algorithm, concerning energy saving, a new metrics, called F_{er} factor was involved. Simulation results, for five different types of input signal statistics, show that energy saving per conversion cycle of up to 25 % can be achieved using the proposed algorithms.

REFERENCES

[1] R. van de Plashe, *CMOS Analog-to-Digital and Digital-to-Analog Converters*, Kluwer Academic Publishers, Boston, 2003

[2] J. Baker, *CMOS Circuit Design, Layout, and Simulation*, IEEE Press, Piscatoway, N.J. 08855, 2005.

[3] B. Razavi, *Principles of Data Conversion System Design*, IEEE Press, Piscataway, NJ, 1995.

[4] P. E. Allen, D. R. Holberg, *CMOS Analog Circuit Design*, Oxford University Press, New York, 2002.

[5] M. D. Scott, B. E. Boser, K. S. J. Pister, "An Ultralow-Energy ADC for Smart Dust", *IEEE JSSC*, Vol. 38, No. 7, July 2003, pp. 1123-1129.

[6] M. de Wit, K. –S. Tan, R. K. Hester, "A Low Power 12b Analog-to-Digital Converter with On-Chip Precision Trimming", *IEEE Journal of Solid-State Circuits*, Vol.28, No. 4, April 1993, pp. 455-461.

[7] T. Kugelstadt, "The Operation of the SAR-ADC Based on Charge Redistribution", *Texas Instruments Analog Applications Journal*, Feb. 2000, pp. 10-12

[8] J. L. McCreary, and P. R. Gray, "All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques – Part I", *IEEE of JSSC*, Vol. SC-10, No.6, December 1975, pp. 371-379.

[9] R. E. Suarez, P. R. Gray, D. A. Hodges, "All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques – Part II", *IEEE of JSSC*, Vol. SC-10, No.6, December 1975, pp. 379-385.