Delay Locked Loop with Linear Delay Element

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Abstract – **Delay Locked Loops (DLLs) and Phase Locked Loops (PLLs) are used in synchronous digital systems in order to improve timings, i.e. to minimize negative effects of skew and jitter in the clock distribution network. In this paper, we propose an efficient DLL architecture implemented with linear delay element. Linearization is achieved by modifying the classical hardware structures of the bias and charge pump circuits [1]. Namely, in our proposal both circuits, instead of single ended use differential input/output structure. This allows us to realize process independent and temperature compensated DLL circuit. Simulation results, that relate to models of 1.2 mm CMOS double-poly double-metal technology, show that the proposed DLL has linear delay regulation and stable lock-in for supply voltage, temperature, and parameter's technology process variations, in the full range of regulation.**

Keyword – **DLL, CMOS circuits design, delay.**

I. INTRODUCTION

Correct timing is necessary for proper operation of high-performance digital and mixed-signal circuits. As the size and operating frequency of VLSI systems increase, designing of clock distribution system poses numerous challenges. In general, the quality of clock pulses is determined by several factors such as frequency, phase, duty-cycle, jitter, and clock skew. A good design solution is one that minimizes all previously mentioned negative effects issues.

Traditionally, PLLs are used for high-frequency clock synthesis. When frequency multiplication is not required, a DLLs offer better performance in respect to PLLs, since its design is easier, and immunity to on-chip noise and stability is better. DLL with installed first-order loop filter is more stable then higher-order PLL. In addition, jitter accumulation makes PLLs more susceptible to power-supply and substrate noise in respect to DLLs [4].

Here we propose an efficient design solution of DLL circuit that is used as a low-jitter clock-source for sigma-delta converter. The DLL structure is based on a linear delay element. Wide-range of delay-regulation in term of control voltage is achieved.

This paper is organized as follows. Section 2. deals with an overview of existing DLLs. Section 3. describes the new proposal. Details that relate to realization of the bias circuit, differential charge pump, and dynamic phase detector are given in Section 4. HSpice simulation results are presented in Section 5. Finally, the conclusion is given in Section 6.

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II. DLL ARCHITECTURE

According to the principle of phase shift generation DLL architectures can be classified into three classes: analog [1], digital [2], and hybrid, usually referred as dual loop [3].

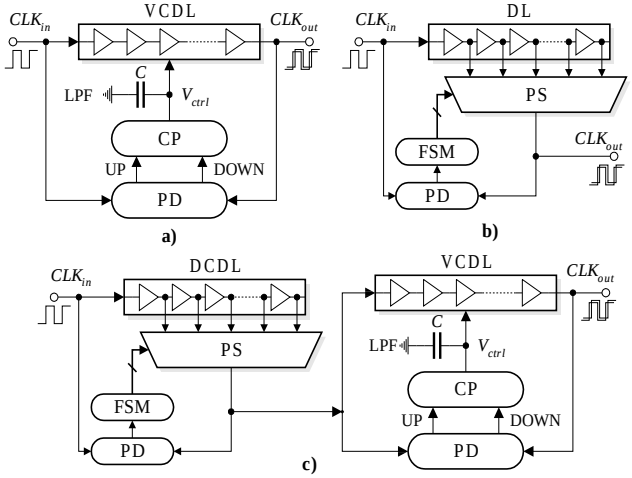

Fig.1. Three classes of DLL architecture

Constituents of the analog DLL, pictured in Fig. 1a), are: Voltage Controlled Delay Line (VCDL), Phase Detector (PD), Charge Pump (CP), and first order Low-Pass Filter (LPF). The VCDL is composed of several variable delay elements connected in cascade. The reference clock CLK_{in} drives the input of VCDL. In order to determine the phase alignment error, the PD compares the rising edges of CLK_{in} and CLK_{out}. Composition of CP and LPF act as an integrator, and generates a control voltage, V_{ctrl}. Under normal condition, the DLL forces to align a phase difference between CLK_{out} and CLK_{in}. When correctly locked, the total delay of VCDL should be equal to one period of the reference clock, CLK_{in}. Analog DLLs are suitable for fine-grain delay variation. They are efficient in applications where small, accurate, and precise amount of delay is necessary to achieve.

The digital DLL shown in Fig. 1b) consists of: Digitally Controlled Delay Line (DCDL), Phase Selector (PS), Phase Detector (PD) and Finite State Machine (FSM). DCDL is implemented as a delay elements chain of variable length. The number of elements in a chain determines the amount of the delay. The PS is realized as a multiplexer. At its output pulse of defined phase-shift (delay) is selected [2]. FSM's output defines the amount of a delay. Delay elements, in DCDL, provide fixed and quantized time delays, and they are used for coarse-grain delay variation in a wide range of regulation. This means that the digital DLL quantizes the clock signal into several coarse-grain discrete delay steps.

The dual-loop DLL, sketched in Fig. 1c), is composed as a series of digital and analog DLL [3]. In general, the dual-loop DLL provides a wide operating phase-shift range. Jitter performance is not good enough, because clock propagation

path includes two loops with a large number of delay elements. Hardware complexity and power consumption of dual-loop DLL are high [4].

III. Proposal: Modified DLL Architecture

Our primarly goal is to design a narrow band low-jitter DLL circuit. According to the previous discussion, we choose an analog DLL architecture as candidate architecture for our proposal. The first step relate now to design of a voltage controlled delay element. The simple structure and relatively wide delay's regulation range were parameters that cause to select a current starved delay element as a good solution for this purpose [1]. However, the main disadvantage of the current starved delay element represents its non-linear delay in function of a control voltage, and is given by the following formula [5]

$$t_{delay} = \frac{C}{I_{cp}} V_{sw} \qquad (1)$$

where: C is load output capacitance, I_{cp} corresponds to charging/discharging current of C, and V_{sw} is a clock buffer (inverter) swing voltage (for more details see Fig. 4b.).

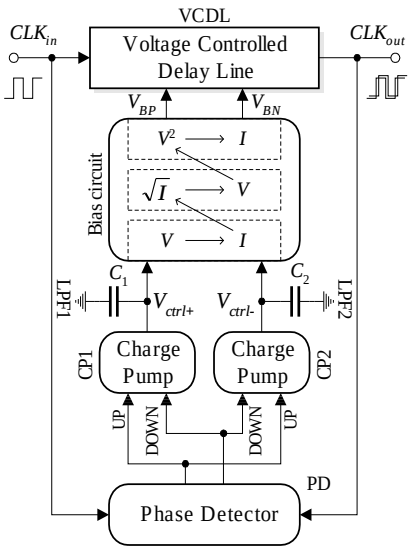

Fig. 2. DLL block scheme

Crucial building block of the delay element is a bias circuit, since it defines the current I_{cp}. Usually, the bias circuit has linear transfer function (I_{cp} vs. control voltage), so concerning formula (1) it involves non-linear delay variation in term of control voltage. Our idea now is to make the variation of I_{cp} to be non-linear, what can be achieved by modifying the bias circuit. As a result, a cascode connection of two non-linear elements, the bias circuit and the current starved delay element, will characterize linear transfer function (delay in term of control voltage).

We adopt realization in which the non-linear bias circuit is based on the square-law characteristic of a MOS transistor in saturation [6]. Let note, that the bias circuit as linear stage is critically sensitive to technology process, supply voltage and temperature variations. In order to make the bias circuit resistant to these variations, we decided to implements it as a differential input-output stage. The differential input control voltage $V_{ctrl}=V_{ctrl+} - V_{ctrl-}$ is obtained by using dual charge pump CP1–CP2 with cross-connected UP/DOWN input signals. Block scheme of the proposed DLL is given in Fig. 2.

IV. DLL Components

A. Delay Line

The delay line, pictured in Fig. 3, consists of four stages. Each stage is composed of a voltage controlled delay element, $VCDE_i$, and an output buffer, OB_i, i = 1,..,4. VCDEs are implemented as standard current starved delay elements, (see Fig. 4b), while OBs are realized with two large inverters connected in cascode. The bias circuit is constituent of the delay line.

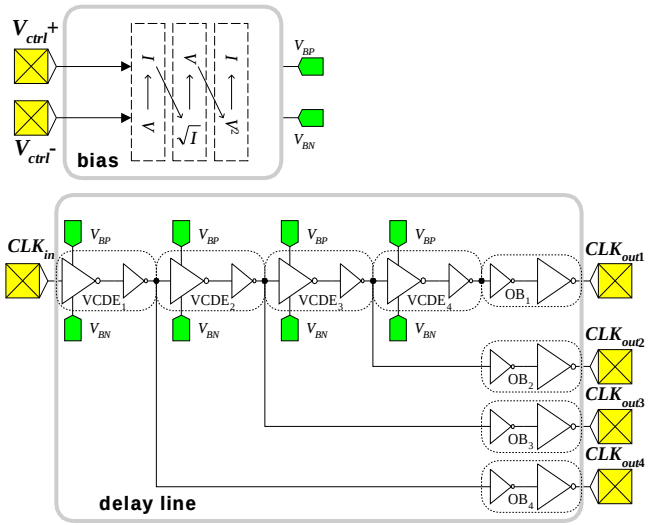

Fig. 3. Four–stage delay line scheme

At its input the bias circuit is driven by a differential control voltage, V_{ctrl}, while at the outputs it generates bias voltages, V_{BP} and V_{BN} (see Fig. 3). Directly, V_{BP} and V_{BN} provide DC operating conditions for inverter's current transistors, M_2 and M_3, while indirectly they determine the charging/discharging current, I_{cp}, of a parasitic inverter's load capacitor C.

Transistors M_{D1} and M_{D2} are parts of the differential input stage. A band-gap based current source I_0' (I_0")=12.5μA supplies a differential stage. Output currents I_1 and I_2, are defined by the following relations

$$I_1 = I_0^{'} + \frac{V_{diff}}{R} \quad \text{and} \quad I_2 = I_0^{''} - \frac{V_{diff}}{R} \qquad (2)$$

where R is a resistor connected between sources of transistors M_{D1} and M_{D2}, and $V_{ctrl} = V_{ctrl+} - V_{ctrl-}$.

According to Eq. (2), we conclude that a linear dependence exists between the input voltage V_{ctrl} and output currents I_1 and I_2, respectively.

Transistors M_{A1} and M_{A2} act as active load resistors and their voltages V_{B1} and V_{B2} are defined as

$$V_{B1} = \sqrt{\frac{I_1}{k_n}} + V_{tn} \quad \text{and} \quad V_{B2} = \sqrt{\frac{I_2}{k_n}} + V_{tn} \qquad (3)$$

The voltage V_{B1} drives the stage composed of transistors M_{s1}, M_{s2} and M_{s3}. At the outputs of this stage two voltages,

V_{BP} and V_{BN}, that are used for polarization of current starved delay elements, are generated.

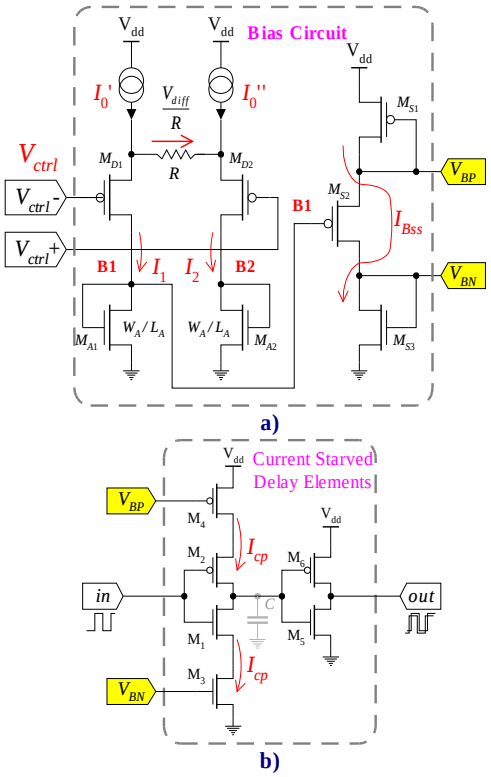

Fig. 4. Bias and VCDL circuits

The current I_{Bss} that flows through transistors M_{s1}, M_{s2} and M_{s3}, see Fig. 4a, is equal to I_{cp}. In this way, the interconnection of the bias stage and the delay element forms two pairs of current mirrors (transistors M_{s1} (M_{s3}) and M_2 (M_3)). The current I_{cp} is defined by the following formula

$$I_{cp} = \frac{k_p}{4}\left(V_{dd} - 2V_{tp} - V_{tn} - \sqrt{\frac{I_1}{k_n}}\right)^2 \qquad (4)$$

Eq. (4) can be represented in the following form

$$I_{cp} = A + B\cdot\sqrt{I_1} + C\cdot I_1 \qquad (5)$$

where constants A, B and C are equal to

$$A = \frac{k_p}{4}\left(V_{dd} - 2V_{tp} - V_{tn}\right)^2,\ B = -\frac{k_p}{4}\frac{2\left(V_{dd} - 2V_{tp} - V_{tn}\right)}{\sqrt{k_n}},\ C = \frac{1}{4}\cdot\frac{k_p}{k_n}.$$

Let note that Eq. (5) approximates a reciprocal relation between the current I_{cp} and the control voltage V_{ctrl}.

B. Dynamic Phase Detector

The phase detector, as a constituent of DLL, has major influence on time delay accuracy of output pulses. Bearing this in mind we propose here an implementation of high-precision dynamic phase detector. Circuit diagram of the dynamic phase detector, used in our case, and described in Reference [1] is pictured in Fig. 5a. Ilustration only the principle of operation of this circuit in given in Fig. 5b. As can be seen from Fig. 5b when the signal BACK leads in respect to signal REF the output is active, in oposite the signal UP is active. Pulse–width of UP (DOWN) pulse is proportional to the phase difference of input signals REF and BACK.

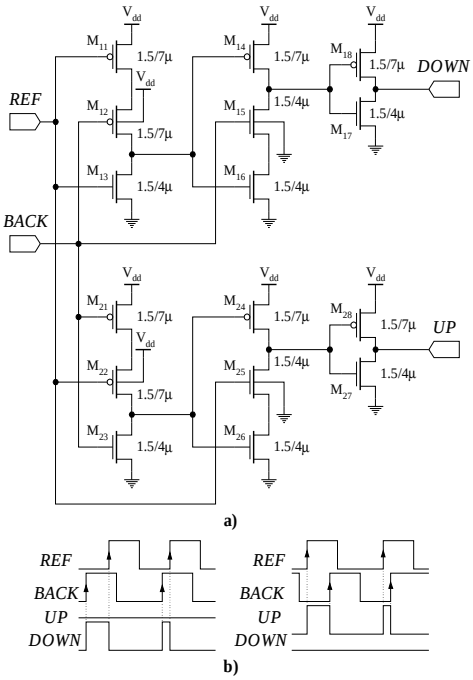

Fig. 5. Phase detector

B. Charge Pump

The charge pumps, CP1 and CP2, charge/discharge capacitors C1 and C2 of low-pass filters LPF1 and LPF2 respectively, see Fig. 2. The differential control voltage V_{ctrl}=V_{ctrl+}–V_{crtl-} (see Fig. 2.) determines a delay of the voltage controlled delay line. The structure of both CP1 and CP2, that act as complementary pair charge pumps, is given in Fig. 6, and is described in detail in Reference [1].

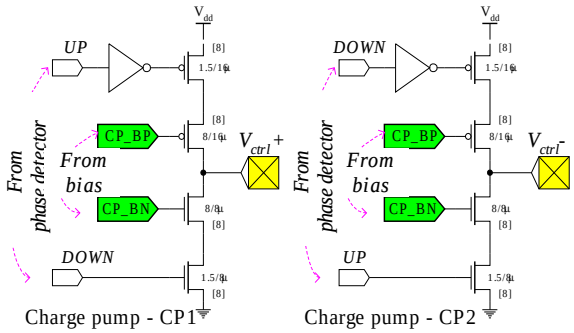

Fig. 6. Differential charge pump

V. DLL SPICE SIMULATION

The design of a bias circuit was verified using HSpice simulation. Models of level 47 that correspond to 1.2µm CMOS technology, were used. During simulation, the supply voltage V_{dd} was fixed to 5V while the temperature T was held at 27°C. Simulation results that relate to I_{cp}=f (V_{ctrl}) and E_{Ap}=F(V_{ctrl}) are presented in Fig. 7.

According to simulation results presented in Fig. 7, we can conclude the following: Reciprocal relation between Icp and V_{ctrl} exists. This possibility allows to achieve a global DLL linear transfer function, i.e. VCDL's delay–versus–control voltage characteristics is linear. The relative approximation

error E_{Ap}, see Fig. 7b, is less then 1%, when the control voltage is within a range of ±0.8V.

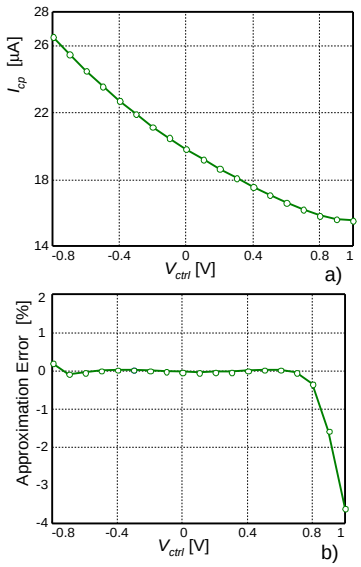

Fig. 7. HSpice simulation of bias circuits

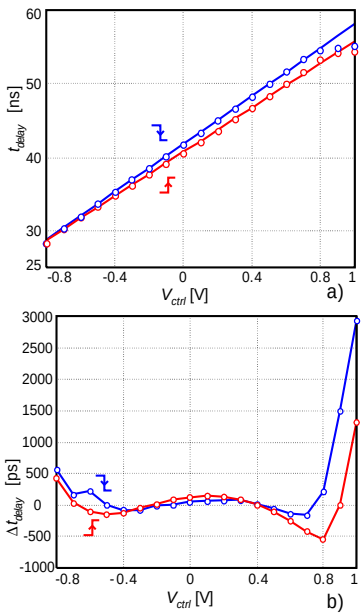

Fig. 8. Simulation of delay t_{delay} in term of control voltage V_{ctrl}

HSpice simulations results that correspond to the delay line are presented in Fig 8. Delays for both leading and trailing clock edges, in term of control voltage, are pictured in Fig. 8 a). The non-linear absolute error, in function of the control voltage, is presented in Fig. 8 b.

From Fig. 8a, we conclude that t_{delay} varies between 28 and 55 ns. This means that the delay line well be operative within the frequency range from 18 to 35MHz. In addition, when the control voltage V_{ctrl} varies in the range of ±0.8V the linearity error is less then 500 ps (see Fig. 8 b).

Fig. 9, deals with HSpice simulation that relate to dynamics of establishing a stable state of the DLL circuit. In the upper part of Fig. 9, input and output clock signals, CLK_{in} and CLK_{out}, are sketched. At its lower part, waveforms that are obtained at the outputs of the phase detector, such as UP and DOWN and V_{ctrl} (V_{ctrl+} and V_{ctrl-}), are given. The looking state is characterized as instant when: a) Full agreement between clock signals, CLK_{in} and CLK_{out}, exists; b) UP and DOWN signals disappear, and; c) control voltages V_{ctrl+} and V_{ctrl-} are of constant values. The elapsed time, from the start to establishing a stable looking state, is approximately 300ns.

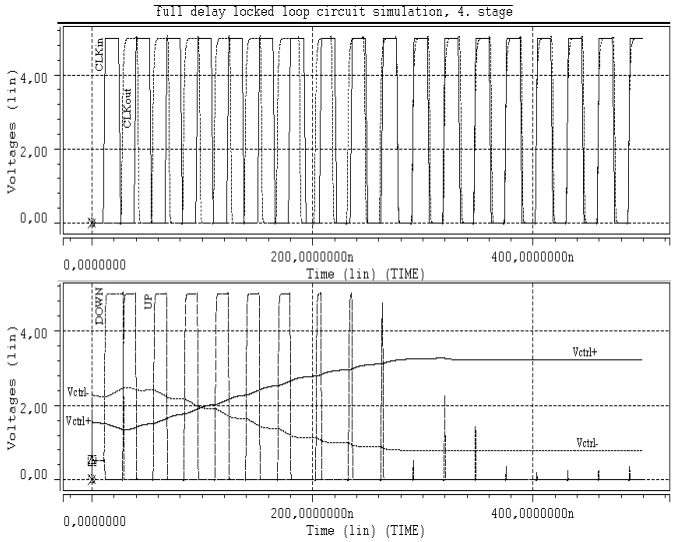

Fig. 9. DLL transient HSpice simulation

VI. Conclusion

In this paper, we describe an implementation of a DLL with linear voltage controlled delay elements. Linearization is achieved by modifying the hardware structures of the bias and charge pump circuits. In our proposal, both circuits use differential input/output structure. This allows us to realize process independent and temperature compensated DLL circuit. HSpice simulation results for 1.2µm CMOS technology high delay linearity (<500 ps) within the full range of regulation (from 28 to 55 ns) and stable lock-in for supply voltage, temperature, and technology process variations, is achieved.

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