PULSEWIDTH CONTROL WITH DELAY LOCKED LOOP

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***Abstract*-- The duty-cycle of a clock, within the VLSI IC, is liable to be changed when the clock passes through several buffer stages in the multistage clock buffer design. The pulse-width may be changed due to unbalance of the *p* and *n* MOS transistors in the long CMOS buffer. This paper describes a delay locked loop with double edge synchronization mainly used in a clock alignment process. SPICE simulation results, that relate to 1.2 mm CMOS technology, shown that the duty-cycle of the multistage output pulses can be precisely adjusted to (50±0.8)% within the operating frequency range, from 55 MHz up to 166 MHz.**

***Index terms*-- dll, duty cycle corrector, delay line**

1. INTRODUCTION

Almost all complex synchronous CMOS digital VLSI ICs rely on clock pulses to control data transfer. In order to reach a highest circuit speed, the clock distribution system must be carefully designed. A great deal of attention has been paid to clock recovery, clock regeneration, timing, and distribution [1].

Automatic control techniques, such as Phase-Locked Loop (PLL) and Delay-Locked Loop (DLL) have been widely used in high-speed clock alignment applications such as double-data rate (DDR) SDRAMs, pipelined microprocessors, network processors, etc. [2].

In a PLL implementation the chip has its own reference clock oscillator (VCO) that is phase-locked to an external reference clock. In general, a PLL clock aligner is superior in applications where noise on the reference clock dominates, and self-induced jitter within the VCO is negligible. On the other hand, a DLL provides superior performance when a clean reference clock is available. A DLL is commonly used to lock the phase of the buffered clock to that of the input data. Typically, we meet this in applications where no clock synthesis is required, such as often the situation for multi-chip digital systems with well-designed system clock distribution network [2].

In high-speed design a multistage clock buffer implemented with a long inverter chain is often needed to drive a heavy capacitive load. For these designs, as well as for applications in which the timing of both edges of the clock is critical [10], it is difficult to keep the clock duty cycle at its ideal value 50 %, primarily due to various asymmetries in signal paths and unbalances of the *p* and *n* transistors in the long buffer. As a consequence the clock duty cycle will deteriorate from 50 %, and in the worst case, the clock pulse may disappear inside the clock buffer, as the pulse width becomes too narrow or too wide [6-9].

Duty-cycle distortion is usually addressed in PLLs by simply running the PLL's VCO at twice the system frequency and using a post divider triggered on one edge of the VCO output to produce the output clock of the PLL. This ensures good 50 % duty cycle. In a DLL, however no frequency multiplication is possible. Therefore, the duty-cycle of the output signal must be corrected to 50 %. A conventional solution is to attach duty-cycle correction circuit to the clock output driver with the price of added area [4].

In this paper, we describe a new structure of a DLL circuit with clock alignment capability of both leading and trailing output pulse edges. This circuit can be used to obtain correct the duty-cycle factor (50 %) in a multistage clock buffer.

2. DLL WITH DOUBLE EDGE SYNCHRONIZATION

The structure of the proposed Delay Locked Loop with Double Edge Synchronization (DLL–DES) clock alignment circuit is pictured in Fig. 1. The click aligner is composed of a voltage controlled delay line, VCDL, two phase detectors, PD1 and PD2, two charge-pumps, CP1 and CP2, two first

order low-pass filters, LP1 and LP2, and a multistage clock buffer, CB. The negative feedback in the loop adjusts the delay through the VCDL by integrating the phase shift errors that result between the periodic reference input, CLK_{in}, and the multistage output, CLK_{out}.

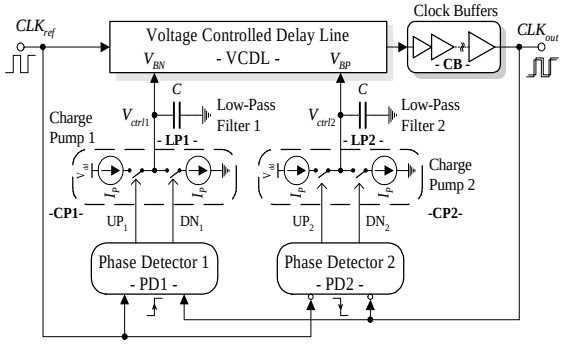

Fig. 1. DLL's architecture with double edges synchronization

The underlying idea for this approach is to provide delay regulation for both a rising and trailing edge of the output clock pulse CLK_{out}. For implementation of variable delay regulation the building block VCDL is used. The control voltage V_{BN} (V_{BP}) defines delay regulation of a rising (trailing) clock pulse edge. The phase detector PD1 (PD2) compares phase shifts of rising (trailing) edges between the input, CLK_{in}, and output, CLK_{out}, clock pulses. UP1 (UP2) pulses cause I_p to add charge to loop filter capacitor C, whereas DN1 (DN2) pulses remove charge. The LP1's (LP2's) output, V_{ctrl1} (V_{ctrl2}), is connected to the VCDL control input at node V_{BN} (V_{BP}). When the system, from Fig. 1, enters in stable state both edges of CLK_{out} are synchronized and phase shifted in respect to the referent clock CLK_{in}. An important feature of this architecture is that the duty-cycle of CLK_{out} is maintained at value of 50 %.

3. EQUIVALENT MODEL OF DLL-DES: TRANSFER FUNCTION AND PULSE-WIDTH

The equivalent model of a DLL-DES is pictured in Fig. 2. It is decomposed into two independent control loops, DLL-R and DLL-F. The upper one, DLL-R, determines a time delay of the output rising edge, while the lower, DLL-F, define the time delay of falling edge. Both control loops are of almost identical structure. The differences are the following:

i) The phase detector PD1 is sensitive to a rising, while PD2 to a falling pulse edge;

ii) The voltage controlled delay line VCDL-R defines the time delay of a rising output pulse edge, while VCDL-F of the falling edge.

The building block CP1 has identical transfer function as CP2. The transfer functions of constituents LP1 and LP2 are identical, too.

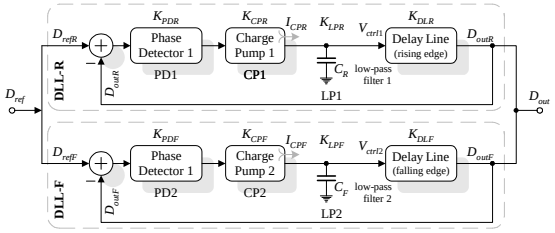

Fig. 2. Equivalent model of DLL-DES.

Having in mind that the delay alignment is performed independently for the rising and falling edge, in the analysis that follows, we assume that DLL-DES's operation can be described as independent activities of two separate loops. Our analysis is based on frequency response of the DLL and is similar to that one described in [11]. Accordingly, for the upper loop, the output pulse delay $D_{outR}(s)$, is related to the input delay, $D_{refR}(s)$, by

$$D_{outR}(s) = \left(D_{refR}(s) - D_{outR}(s)\right) \cdot k_{PDR} \cdot k_{CPR} \cdot k_{LPR} \cdot k_{DLR} \quad (1)$$

where:

$k_{PDR} = \frac{dDC_{PDR}}{dD} = \frac{1}{T_{ref}}$ – corresponds to phase detector sensitivity;

$k_{CPR} = \frac{dI_{CPR}}{dDC_{PDR}} = I_{CPR}$ – charge pump current sensitivity;

$k_{LPR} = \frac{dV_{ctrl1}}{dI_{CPR}} = \frac{1}{sC_R}$ – loop filter transfer function;

and

$k_{DLR} = \frac{dD}{dV_{ctrl1}}$ – delay line sensitivity,

with: f_{ref} – frequency of the referent clock, CLK_{ref}; T_{ref} – time period of referent clock; DC – duty-cycle of PD1's output at f_{ref}; $D = D_{outR} - D_{refR}$ – delay difference; I_{CPR} – output charge pump current; and C_R –filter capacitance.

By rearranging Eq. (1), for the DLL's closed loop transfer function, $H_{DLLR}(s)$, we obtain

$$H_{DLLR}(s) = \frac{D_{outR}(s)}{D_{refR}(s)} = \frac{k_{PDR} \cdot \frac{k_{CPR}}{sC_R} \cdot k_{DLR}}{1 + k_{PDR} \cdot \frac{k_{CPR}}{sC_R} \cdot k_{DLR}} = \frac{1}{1 + s \cdot \frac{C_R}{k_{PDR} \cdot k_{CPR} \cdot k_{DLR}}} = \frac{1}{1 + \frac{s}{w_{NR}}} \quad (2)$$

where $w_{NR} = \frac{k_{PDR} \cdot k_{CPR} \cdot k_{DLR}}{C_R} = \frac{f_{ref} \cdot I_{CPR} \cdot k_{DLR}}{C_R}$ represents a pole of the DLL's transfer function.

By analyzing Eq. (2) we conclude that the DLL has first order transfer function and the frequency of its pole corresponds to a loop bandwidth.

The delay at the DLL-DES's output can be determined according to the transfer function which is obtained using an identical approach as one for conventional DLL architecture. Concerning the rise pulse edge, a transfer function has the form defined by Eq. (2). Accordingly the delay of a rising edge is defined by

$$D_{outR}(s) = H_{DLLR}(s) \cdot D_{inR}(s) = \frac{1}{1+\frac{s}{w_{NR}}} \cdot D_{inR}(s) \quad . \tag{3}$$

For the transfer function of the falling edge, $H_{DLLF}(s)$, we have

$$H_{DLLF}(s) = \frac{D_{outF}(s)}{D_{inF}(s)} = \frac{1}{1+\frac{s}{w_{NF}}} \tag{4}$$

where $w_{NF} = \frac{f_{ref} \cdot I_{CPF} \cdot k_{DLF}}{C_F}$.

The delay of a falling edge is

$$D_{outF}(s) = H_{DLLF}(s) \cdot D_{inF}(s) = \frac{1}{1+\frac{s}{w_{NF}}} \cdot D_{inF}(s) \quad . \tag{5}$$

The pulse-width W_{ref} and W_{out} of the reference clock, CLK_{ref}, and from the DLL-DES's output, CLK_{out}, (see Fig. 2) are defined as $W_{ref} = D_{inR} - D_{inF}$ and $W_{out} = D_{outR} - D_{outF}$, respectively.

The pulse-width of the DLL-DES's output depends on a difference between D_{outR} and D_{outF} and is defined as

$$W_{out}(s) = D_{outR}(s) - D_{outF}(s) = \frac{1}{1+\frac{s}{w_{NR}}} \cdot D_{inR}(s) - \frac{1}{1+\frac{s}{w_{NF}}} \cdot D_{inF}(s) \tag{6}$$

Due to symmetry in the DLL-DES, i.e. identical realizations of the upper and lower branch in the circuit model presented in Fig. 2, the following is valid, $\omega_{NR} = \omega_{NF} = \omega_N$. Accordingly, Eq. (6) can be written as

$$W_{out}(s) = \frac{1}{1+\frac{s}{w_N}} \cdot \left(D_{inR}(s) - D_{inF}(s)\right) = \frac{1}{1+\frac{s}{w_N}} \cdot W_{ref}(s) \tag{7}$$

Finally the transfer function $H_W(s)$ which defines the ratio between the output and input pulse-width is given as

$$H_W(s) = \frac{W_{out}(s)}{W_{ref}(s)} = \frac{1}{1+\frac{s}{w_N}} \tag{8}$$

By analyzing Eq. (8) we can conclude that the DLL-DES is:

- first order system,
- always stable, and
- the duty-cycle of the referent input, CLK_{ref}, and output pulse, CLK_{out}, is identical, an is equal to 50%.

4. CIRCUITS IMPLEMENTATION

In the sequel we will describe, in more details, the structure and principle of operation of each constituent of a DLL-DES based clock aligner.

3.1. Voltage controlled delay line

The actual implementation of a VCDL is comprised of a number of cascaded variable delay buffers. Each delay buffer (adjustable timing element) is of identical structure. Current starved delay element (CSDE) was chosen as a convenient candidate for realization of the delay buffer. The main design decision for such a choice was the following: CSDE provides independent delay regulation of both rising and falling clock pulse edges. Independent delay regulation can be achieved by varying the current of *p* and *n* MOS transistors.

In conventional CSDE (see Fig. 3(a)) a single control voltage V_{ctrl}, generated by a bias circuit, modulates the on resistance of pull-down M_3, and through a current mirror, pull-up M_4 [5]. The variable resistances control the current available to charge or discharge the parasitic load capacitance.

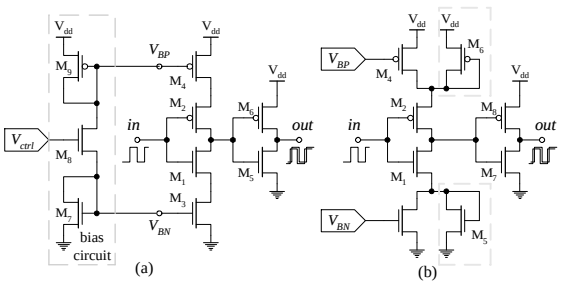

Fig. 3. Modified current starved delay element

In order to achieve independent, instead of single, variable resistances control, we propose here a modified version of CSDE, as one given in Fig. 3(b). In our approach, both control voltages, V_{BN} and V_{BP}, directly drive gates of M_3 and M_4 MOS transistors, respectively. Transistors M_5 and M_6 act as symmetric loads and are used for two purposes: a) to linearize a voltage-to-delay transfer function of the CSDE; and

b) provides correct initial condition for DLL operation even in a case when both control voltages V_{BN} and V_{BP} are out-of-regulation limits (for example, M_4 and M_3 are switched off). The modified CSDE was designed for 1.2μm CMOS technology, for 5V power supply voltage. A SPICE simulation results that correspond to delay functions of both rising and falling pulse edges are given in Fig. 4. The obtained results in Fig. 4 show that linear regulation of voltage-versus-delay can be achieved. In general, CSDE offers good delay line stability in respect to temperature and supply voltage variations. Its main disadvantage is relatively limited range of delay regulation, i.e. low-sensitivity.

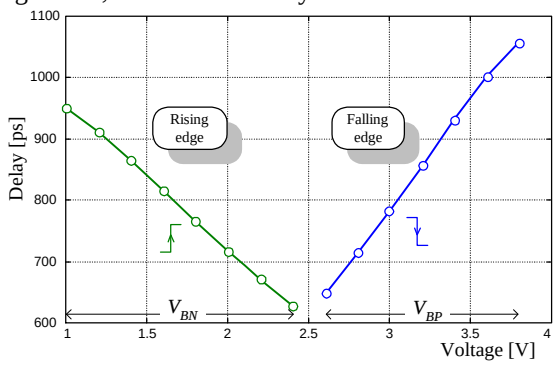

Fig. 4. Rising and Falling edge delay in term of control voltages

3.2 Phase detector

The phase detector measures the phase difference between the time reference and the delay chain. High precision dynamic phase detection circuit based on true single phase logic [3] is adopted in our design. The main advantages of this circuit are simple hardware structure, high-speed of operation, and small dead zone [5]. The UP*x* and DN*x* (*x* refers to 1 or 2) are used to control the charge-pump circuit CP*x*. The PD1 (PD2) is sensitive to rising (falling) clock pulse edge. A modification, in respect to standard solution [5], is performed by substituting MOS transistors P_{12}, N_{12}, P_{22}, and N_{22} (see Fig. 5 (a)) with complementary ones N_{11}, P_{13}, N_{21}, and P_{23} (see Fig. 5(b), respectively.

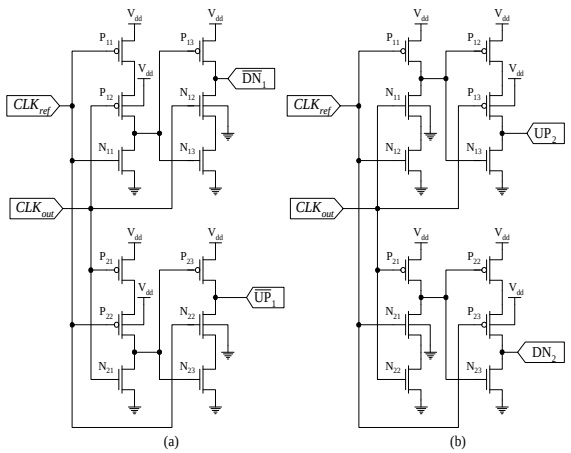

Fig. 5. Implementation of phase detectors for (a) raising and (b) falling edges

Operational principles of PD1 and PD2 are shown in Fig. 6. The widths of UP and DN signals are proportional to the phase difference of the input signals. Fig. 6a (6b) shows the operation of PD1 (PD2). Waveforms on the left side of Fig. 6a (6b) correspond to a case when the signal CLK_{out} (see Fig. 2) leads in respect to the signal CLK_{ref}. Otherwise, timing diagrams on the right side are valid (CLK_{ref} leads the CLK_{out} signal).

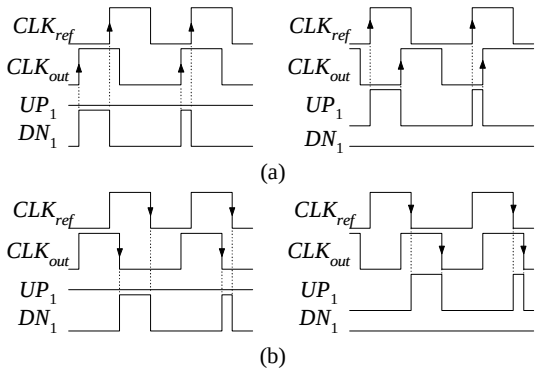

Fig. 6. Waveforms of input and output signals for (a) phase detector 1 and (b) phase detector 2

3.3 Charge pump and loop filter

The charge-pump and loop filter structure is presented in Fig. 7. Transistors P_1 and N_1 act as switching elements driven by pulses UP and DN, while transistors P_2 and N_2 are employed as current sink and source, respectively. The charge-pump charges or discharges the filter capacitor, C. The voltage on this capacitor, V_{ctrl} (V_{BP} or V_{BN} in Fig. 2), sets the VCDL stage propagation delay. The charge-pump the realization of an integrator transfer function with no additional active amplifier, resulting in a zero-phase error in steady state. A small capacitor, *C*, is used for the low-pass loop filter. The current level of the charge-pump and the charge delivered/accepted at every rising/falling clock edge transition are set to a small value [5]. This allows the implementation of the loop capacitor on chip.

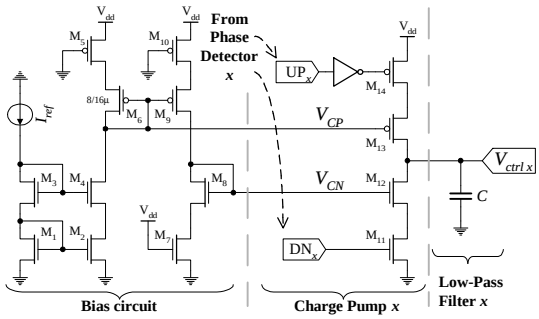

Fig. 7. Current pump and loop filter

The bias circuit provides correct operation of the charge pump. Its structure is given on the left side of Fig. 7. This circuit generates two control voltages, V_{CP} and V_{CN}. These voltages define the charge and

discharge currents of loop capacitor, *C*, that pass through transistors M_{12} and M_{13}.

5. SIMULATION RESULTS

The DES-DLL sketched in Fig. 2 is implemented in 1.2 μm CMOS technology. It is supplied with V_{dd}=5V. SPICE simulation results that relate to referent clock excitation f_{ref}=80MHz are given in Fig. 8. The DES-DLL is operatives within the frequency range from 55 MHz up to 166 MHz.

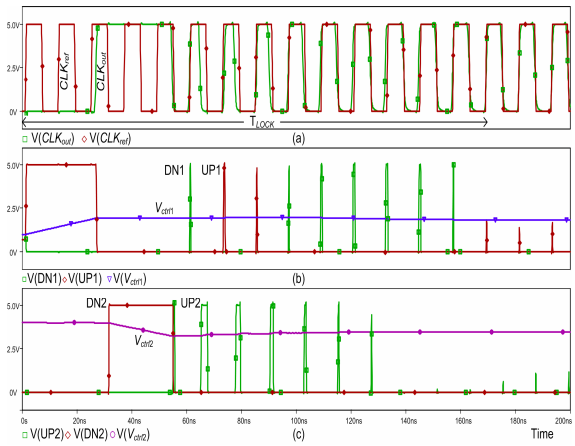

Fig. 8. Simulation of DLL with Double Edges Synchronization

Timing diagrams that correspond to referent input clock pulses, CLK_{ref}, and buffer output, CLK_{out}, are given in Fig. 8(a). This Fig. shows that the locking time, T_{LOCK}, between the referent CLK_{ref} and output CLK_{out} pulses is less than 200ns. We define T_{LOCK} as a time interval starting from initial condition up to the instant when total coincidence of rising and falling edges between both pulses, CLK_{ref} and CLK_{out}, exists, (see Fig. 8(a)). If we assume that CLK_{ref} is symmetrical then the coincidence corresponds to 50% duty-cycle of CLK_{out}.

Fig. 8(b) (8(c)) deals with waveforms that are obtained at the outputs UP1 (UP2), DN1 (DN2), and V_{ctrl1} (V_{ctrl2}). As can be seen from Fig. 8(b) (8(c)) UP*x* and DN*x* signals define the control voltage V_{ctrlx} during the transition period ($0 < t < T_{LOCK}$). After that the system enters in stable state and UP*x* and DN*x* signals disappear and $V_{ctrl\,x}$ takes a constant value.

According to the obtained results we can conclude that the proposed DES–DLL can be seen to have a wide-operational range and good duty–cycle correction capability. According to the obtained results we can conclude that the proposed DES-DLL can be seen to have a wide-operational range and good duty-cycle correction capability. Simulation results presented in Fig. 9 show that, within the full DLL-DES's operating range (55–166 MHz), the duty cycle error is less then 0.8%.

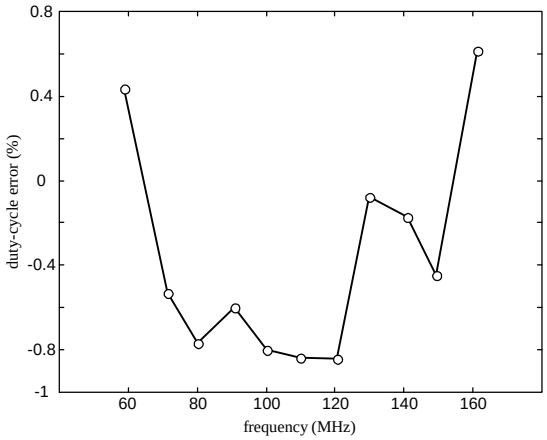

Fig. 9. Duty-cycle error.

6. CONCLUSION

In this paper a new DLL architecture with clock alignment capability of both leading and trailing edges is described. The proposed circuit was simulated using models for 1.2 μm CMOS technology and SPICE simulator. The clock aligner has been designed specifically to correct precisely the duty-cycle factor in a multistage clock buffer to (50±0.8) % within the operating frequency range from 55 MHz up to 166 MHz. Timing diagrams are measured by simulation. The proposed DLL based clock aligner keeps the same benefits of conventional DLL's such as good absolute stability, fast-response, and low-level output jitter for both (rising and falling) edges. Such circuits serve in many applications including clock distribution network within the VLSI ICs, high-speed DRAM, and core-to-core interconnects within a system-on-chip designs.

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