

An adaptive pulse-width control loop

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The clock distribution and generation circuitry forms a critical component of current synchronous digital systems. Digital system clocks must not only have low jitter, low skew, but also well-controlled duty cycle in order to facilitate versatile clocking techniques. In high-speed CMOS clock buffer design, the duty cycle of a clock is liable to be changed when the clock passes through a multistage buffer because the circuit is not pure digital (Fenghao and Svensson 2000). In this paper, we propose a pulsewidth control loop referred as APWCL (Adaptive Pulsewidth Control Loop) that adopts the same architecture as the conventional PWCL, but with two modifications. The first one relates to implementation of the pseudo inverter control stage (PICS), while the second to involvement of adaptive control loop. The first modification provides generation of output pulses during all APWCL's modes of operation and the second faster locking time. For 1.2 μ m double-metal double-poly CMOS process with $V_{dd}=5V$ and operating frequency of 100MHz, results of SPICE simulation show that the duty cycle can be well controlled in the range from 20% up to 80% if the loop parameters are properly chosen.

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1. Introduction

With the rapid advances in deep-submicron CMOS process, modern digital systems operated from hundred kilohertz up to few gigahertz have been successfully developed for several years, such as high-speed high-performance superscalar and VLIW microprocessors, network processors, double data rate SDRAM, and so forth. Since there are more and more functional blocks integrated in the same chip as guided by the concept of system-on-a-chip and system-on-silicon, the skew, jitter, and asymmetric duty cycle clock signal become bottlenecks in realizing high-speed and high-performance digital systems (Flynn *et al.* 1999).

In order to minimize the negative effects caused by skew and jitter of clock signals, phase locked loops (PLLs) and delay locked loops (DLLs) are used (Maneatis *et al.* 2002). From one hand in applications where frequency multiplication is required, PLLs represent good candidate design solutions. From the other hand, when there are cases where no clock synthesis is required, DLLs offer an attractive alternative to PLLs due to their better jitter performance, inherent stability, and simpler design (Yongsam *et al.* 2000).

In systems that adopt a double data rate technology, both rising and falling edges of the clock are used to sample input data. These systems require the duty cycle of the clock to be precisely maintained at 50%. Therefore, an important issue is how to generate a clock with precise 50% duty cycle for high-speed operation (Sung-Rung and Shen-Iuan 2004). Automatic control technology, such as pulsewidth control loop (PWCL) has been widely used for adjusting the output duty cycle of multistage driver for several years and was described by Sung-Rung and Shen-Iuan (2004), Po-Hui and Jinn-Shyan (2002), and Fenghao and Svensson (2000).

In this paper, we address a new approach to achieve a fast-locking PWCL architecture, called APWCL. It can be used to control the pulsewidth in multistage clock buffer. Architectural description and principle of operation for three different types of PWCLs, already well known from literature, covered is in Section 2. Section 3, describes the structure of the proposal, referred as adaptive pulsewidth control loop. The APWCL's principle of operation is described in Section 4. Section 5 deals with analysis and design of the control loop. Details related to APWCL implementation and simulation results are given in Section 6. Section 7 gives a conclusion to this paper with summary.

2. Related works

Clocking is one of the most important decisions facing the designer of a digital system (Oklobdzija *et al.* 2003). A clock signal is used to synchronize different parts of a digital system, and the quality of the clock signal. Frequency, amplitude, phase, and duty cycle, undoubtedly influence the system performance (Po-Hui and Jinn-Shyan 2002, and Öberg 2003). Currently, the PLLs and DLLs are mainly used for aligning frequency and clock phase, while the PWCLs are intended to control the duty cycle of the clock signal generated from a multistage driver (Po-Hui and Jinn-Shyan 2002).

In high-speed design, a multistage clock buffer implemented into a long inverters chain is often needed to drive a heavy capacitive load. It is difficult to keep the clock duty cycle at 50% for these design solutions. When the clock signal passes through a multistage buffer, the symmetrical pulse-width may be destroyed due to the unbalance of the N and P channel transistors in the long buffer. This unbalance is introduced by many factors, such as process deviations, temperature changes, or mismatch in design. Consequently, the clock duty cycle will wonder away from 50%. In the worst case, as the pulsewidth becomes too narrow or too wide, the clock pulse may disappear inside the clock buffer (Fenghao and Svensson 2000).

To overcome these problems, PWCLs have been proposed by Sung-Rung and Shen-Iuan (2004), Po-Hui and Jinn-Shyan (2002), and Fenghao and Svensson (2000). We will give a short review concerning the architecture and principles of operation for all three types of PWCLs, referred as conventional PWCL described by Fenghao and Svensson (2000), fixed-phase PWCL referred by Po-Hui and Jinn-Shyan (2002), and fast-locking PWCL described by Sung-Rung and Shen-Iuan (2004), in the sequel.

2.1. Conventional PWCL

Schematic diagram of the conventional PWCL (Fenghao and Svensson 2000) is pictured in Figure 1. As it can be seen from Figure 1, the conventional PWCL is realized as a system with feedback loop.

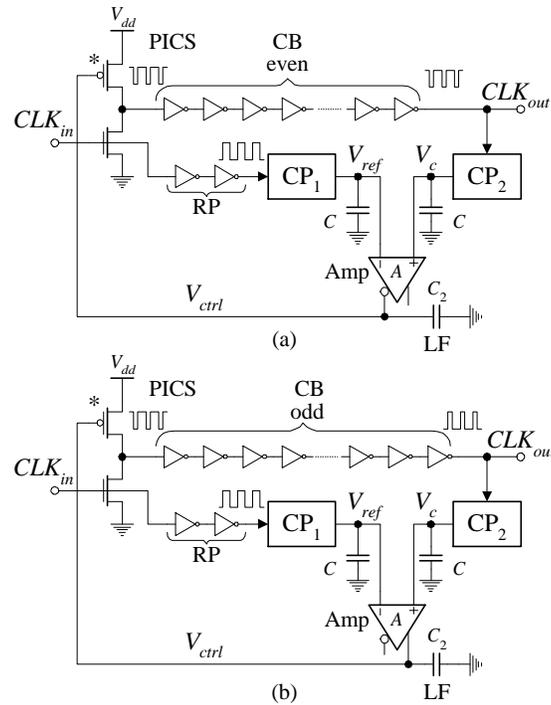


Figure 1. Conventional PWCL: (a) clock buffer with even number of stages;

(b) clock buffer with odd number of stages;

The feedback loop functionally consists of:

- Pseudo-Inverter Control Stage (PICS) - chosen to be the first stage of the clock buffer and functions as a voltage-controlled pulse-generator. By changing the control voltage, V_{ctrl} , we can adjust the pulsewidth of the output clock. PICS is implemented as a simple inverter. Here, mark "*" indicates the controlled transistor;
- Clock Buffer (CB) - a long inverter chain or buffer which acts as a multistage driver. A number of the stages in the clock buffer must meet a condition to guarantee the correct feedback. When the clock buffer has an even (odd) number of the stages the PWCL is configured as in Fig 1a (1b);
- Charge Pump 1 (CP1) - converts pulsewidth into current which charges or discharges capacitor C . At its output, CP1 creates a reference voltage V_{ref} , by connecting to a reference clock with 50% duty cycle;
- Charge Pump 2 (CP2) - is another identical charge pump that creates a voltage V_c , i.e. it steers current by the clock pulse CLK_{out} for detecting the change of pulsewidth;
- Amplifier (Amp) - the amplifier is characterized by its gain A , realized as a differential amplifier. It is intended to provide a certain gain in the loop at low frequency;

- f) Reference Pulse (RP) - two stage inverter buffers used to drive CP1 with 50% duty cycle referent clock pulses;
- g) Loop Filter (LF) - the output resistor of Amp and capacitor C_2 form a first-order low-pass filter.

In Figure 1 two identical single-ended charge-pumps are used. One of them is used for detecting the pulsewidth of the clock being controlled, and another is connected to a standard clock with 50% duty cycle for generating V_{ref} . The voltage V_{ref} is taken as reference voltage. The charge-pumps, CP1 and CP2, and the differential amplifier, Amp, are constituents of the duty cycle comparator. The output voltage V_{ctrl} controls the operation of PICS.

The pulsewidth of CB is controllable. This means that if the CB's clock output deviates from 50% duty cycle, the control voltage, V_{ctrl} , will change so that the offset can be removed. When the loop is stable the CB output is adjusted to 50% duty cycle, and the controllable dynamic range covers the range of possible offset.

The conventional PWCL (Fenghao and Svensson 2000) is a nonlinear feedback loop. The control voltage, V_{ctrl} , must be quite enough to ensure a precise duty cycle as the loop is closed. In order to follow duty cycle variations the loop gain must be kept low, however, with low gain the loop may take a long time to settle. This long settling time reduces the timing budget for other function blocks in a system (Sung-Rung and Shen-Iuan 2004).

2.2. Fixed-phase PWCL

Po-Hui and Jinn-Shyan (2002) propose a similar architecture as the conventional PWCL. The main difference relate to involvement of two new building blocks. Namely, a novel duty cycle detector and voltage controlled pulse generator, that enable higher frequency operation at low-voltage in respect to the proposal given by Fenghao and Svensson (2000), are implemented. The voltage controlled pulse generator consists of NAND gate and two inverter chains. The first chain has fixed, while the second, realized as shunt capacitor delay line, has a variable delay. The duty cycle detector is implemented as a push-pull charge pump. The scheme of the fixed-phase PWCL is given in Figure 2. In order to perform phase locking as well as pulsewidth adjustment simultaneously, the clock buffer can include PLL/DLL and PWCL. Identical problems concerning precise duty cycle generation as one described by Fenghao and Svensson (2000) are typical for the fixed-phase PWCL, too.

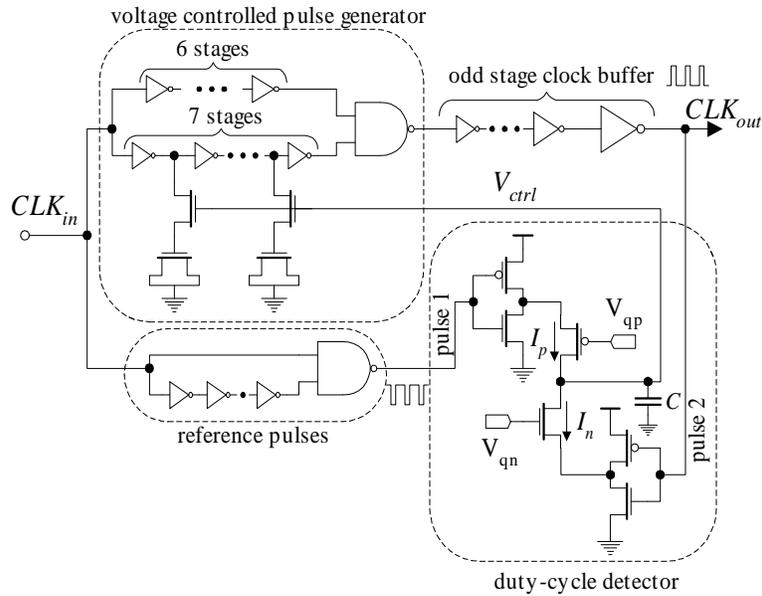


Figure 2. Fixed-phase PWCL.

2.3. Fast-locking PWCL

A 500MHz-1.25GHz fast-locking PWCL (see Figure 3) with presettable duty cycle realized in 0.35 μm CMOS technology is described by Sung-Rung and Shen-Iuan (2004). Fast-locking mechanism is implemented thanks to building blocks enclosed in the area encircled by a dashed line. This part of the electronics consists of a voltage-difference-to-digital-converter (VDDC) and a pair of switched charge pumps (SCP) circuits. The VDDC is used to detect the corresponding linear and nonlinear regions in a transient process, while the SCP circuits provide different charge pump currents corresponding to the control codes from VDDC and the external codes that are used to preset the duty cycle of CLK_{out} . In respect to the conventional PWCL, the fast locking PWCL can reduce the lock time by a factor of 2.58. Duty cycles of the output clocks can range from 35% to 70% in step of 5%.

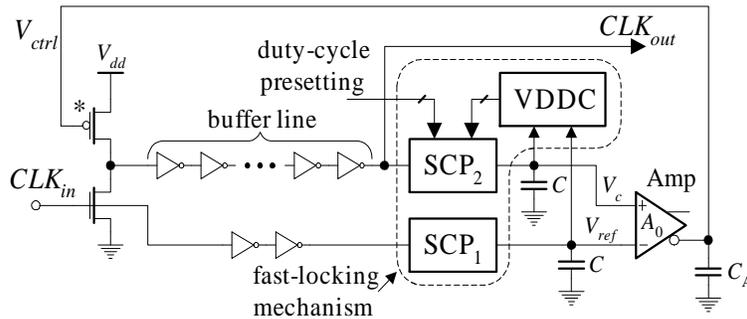


Figure 3. Fast-locking PWCL with presettable duty cycle.

3. Adaptive PWCL

Block diagram of the APWCL is sketched in Figure 4. From functional point of view, the following building blocks can be identified:

- (a) Pseudo-Inverter Control Stage (PICS) – at the output, $PICS_{out}$, pulses of variable duty cycle are generated. V_{ctrl} , is used as an input control voltage;
- (b) Clock Buffer (CB) – an inverter chain implemented as odd (even) stages clock driver;
- (c) Charge Pumps (CPx) – two voltage controlled charge pump circuits, CP1 and CP2, of different structure;
- (d) Reference Pulse (RP) – chain composed of two inverters;
- (e) Bias Circuits (BC1 and BC2) – provide control voltages for transistors polarization of CP1, CP2 and PICS;
- (f) Differential-input differential-output operational amplifier (Amp) – acts as an inverting (non-inverting) amplifier in a feedback control loop. For odd (even) number of stages in CB the Amp is implemented as non-inverting (inverting) amplifier;
- (g) Low-pass filter (LF) – filter element in a feedback control loop;
- (h) Charge Pump Controller (CPC) – is implemented as differential amplifier. At its output, the CPC generates control voltage V_A that is proportional to $V_{ref} - V_c$ on voltage difference.

In respect to the conventional PWCL proposed by Fenghao and Svensson (2000), there are several novelties involved into APWCL. The first one relates to the PICS, while the second to CP2. In addition, two new building blocks, CPC and BC2 are included into APWCL structure. The other constituents, pictured in Figure 4, are of identical (or almost-identical) architectures as those described by Fenghao and Svensson (2000). So, their analysis will be omitted in the text that follows.

The signals CLK_{in} and CLK_{out} are input and output pulse signals of APWCL, respectively. They drive two charge pumps, denoted as CP1 and CP2 (Figure 4). The output voltage V_{ref} (V_c) of the charge pump CP1 (CP2) is directly proportional to the duty cycle of the input signal CLK_{in} (CLK_{out}). Charge pump CP1 (CP2) load capacitor C_{11} (C_{12}) is discharged during the positive pulse period and charged in the rest of the period. The charging and discharging currents are adjusted to be identical. The signal CLK_{in} is selected as a referent one. Its duty cycle is 50%. Therefore, the voltage V_{ref} at the output of CP1 is referent.

Due to influence of different propagation delays of the leading and trailing edges of the clock signal, when it passes through the long chain clock buffer, the duty cycle of the CLK_{out} become unsymmetrical, i.e. different from 50%.

The voltages V_{ref} and V_c drive the differential amplifier (Amp). Voltage V_{ctrl} is generated at the Amp's output. The V_{ctrl} controls operation of the PICS. When the APWCL is in steady-state, the magnitude of control voltage V_{ctrl} causes the duty cycle of the CLK_{out} to be 50%.

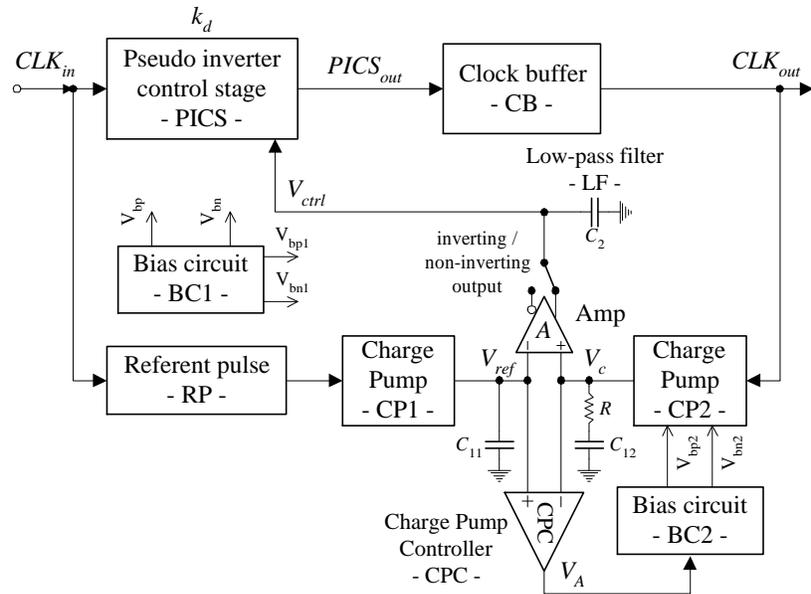


Figure 4. Block diagram of APWCL.

3.1. Pseudo Inverter Control Stage - PICS

An electrical scheme of the PICS is pictured in Figure 5(a). It consists of three N-channel N_1 , N_2 and N_3 , and three P-channel P_1 , P_2 and P_3 , transistors. The PICS's equivalent electrical scheme is presented in Figure 5(b). Transistors P_1 and P_2 act as constant and variable current sources J_1 and J_2 , while transistors N_1 and N_2 operate as constant and variable current sinks I_1 and I_2 , respectively. Transistors P_3 and N_3 belong to the switching parts of the CMOS inverter. Capacitor C_L represents a parasitic capacitive load.

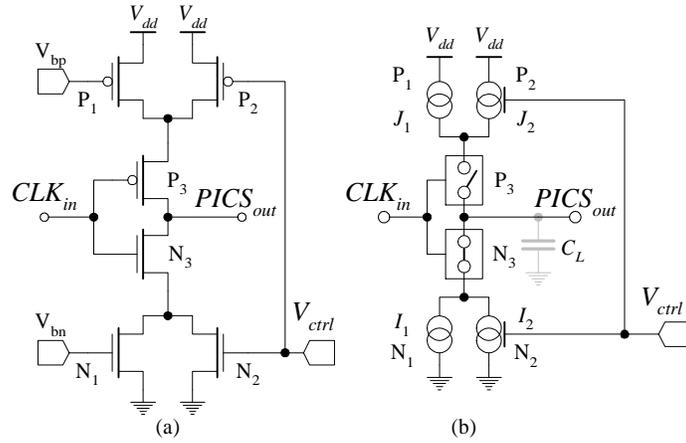


Figure 5. The block PICS: (a) electrical scheme, (b) equivalent scheme.

The amount of the current of the constant current source (sink) J_1 (I_1) indirectly determines the nominal time delay of the leading (trailing) pulse edge at the output $PICS_{out}$. The bias voltage V_{bp} (V_{bn}) is used for polarization of transistor P_1 (N_1). The variable current source (sink) J_2 (I_2) indirectly defines the variable time delay of the leading (trailing) pulse edge. Such a configuration, allows us to achieve controllable time delay for both, leading and trailing pulse edges. Waveforms generated at the output $PICS_{out}$, for different values of the control voltage V_{ctrl} , are shown in Figure 6. As it can be seen from Figure 6, the pulse leading (trailing) edge can vary within the range from t_1 (t_3) up to t_2 (t_4).

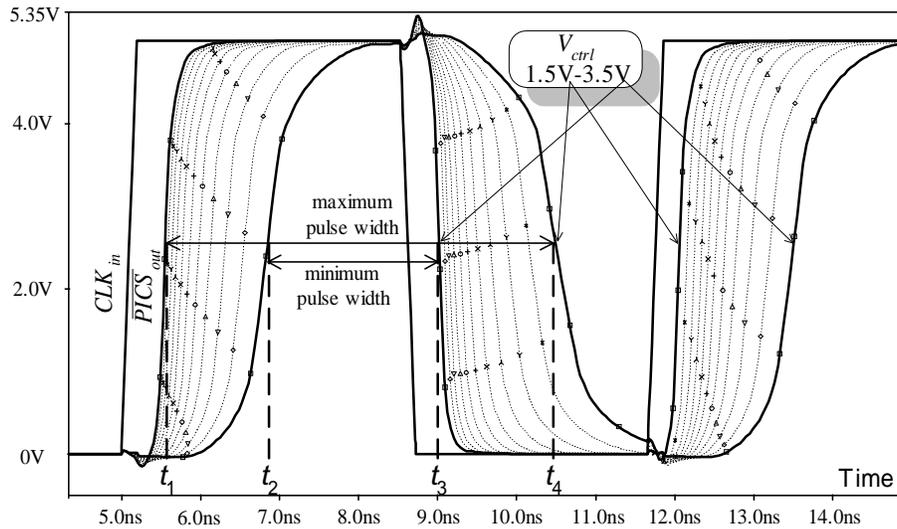


Figure 6. PICS input and output waveforms.

Time delay variation of the leading (trailing) pulse edge, in term of control voltage V_{ctrl} , is presented in Figure 7. For $V_{ctrl}=V_{dd}/2=2.5V$ the time delay for both edges is identical. This means that good symmetry in

geometry between P and N channel transistors is achieved. If the control voltage V_{ctrl} decreases, the time delay of the trailing edge increases while the time delay of the leading edge decreases, and vice versa.

In Figure 8, the range of duty cycle variation, in terms of V_{ctrl} , is shown. Again, duty cycle of 50% for $V_{ctrl}=V_{dd}/2=2.5V$ is achieved. When V_{ctrl} decreases the duty cycle increases, by contraries it decreases.

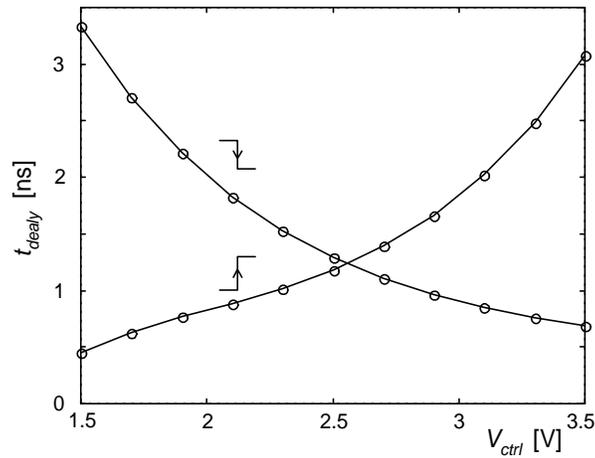


Figure 7. Delay of leading and trailing edges in term of V_{ctrl} .

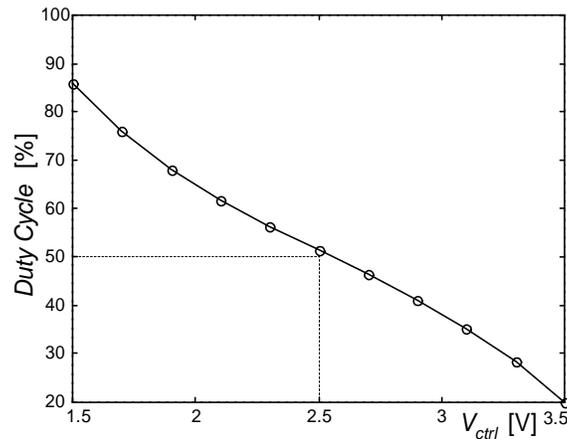


Figure 8. Duty cycle in term of V_{ctrl} .

3.2. Charge pump - CP1

An electrical scheme of the charge pump CP1 is given in Figure 9. The CP1 consists of current source, P_{r2} , and current sink, N_{r2} , transistor, and two complementary switches P_{r1} and N_{r1} . The encircled block BC1 generates two output bias voltage signals, denoted as V_{bp1} and V_{bn1} . These bias voltages are used for polarization of the current source and sink transistors P_{r2} and N_{r2} , respectively.

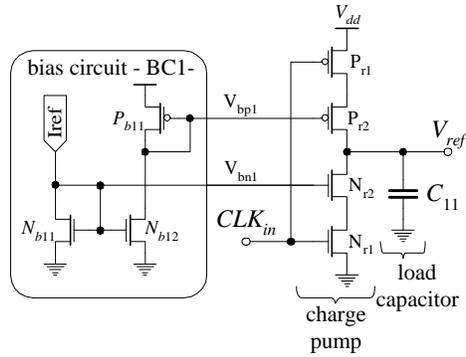


Figure 9. Electrical scheme of CP1 charge pump.

3.3. Parallel charge pump - CP2

The charge pump CP2, pictured in Figure 10, is composed of two charge pumps, CP2₁ and CP2₂, that operate in parallel. The structure of the pump CP2₁ is identical with CP1 (Figure 9). The bias circuit BC2 provides polarization for CP2₂. The block CPC (Figure 4) defines the magnitude of the control voltage V_A .

The load impedance of CP2 is realized as a serial connection of resistor R and capacitor C_{12} . This connection involves one zero in the transfer function of CP2, and also in a transfer function of the APWCL. Involving zero in the APWCL's transfer function allows us to adjust the damping factor x to optimal value ($x=0.707$), and to decrease the transition time in the linear mode during the period of establishment of a steady-state (for more details see section 5).

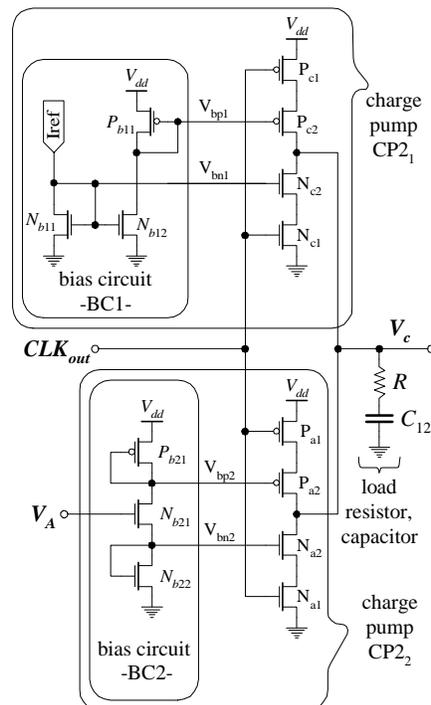


Figure 10. Electrical scheme of CP2 charge pump.

3.5. Voltage controlled bias circuits - BC2

This building block, at its input, accepts the control voltage V_A , and according to its magnitude generates two output control voltages V_{bp2} and V_{bn2} . The output voltages V_{bp2} and V_{bn2} define the source and sink currents, of the charge pump CP2₂, respectively. In order to provide normal operating condition to switch ON/OFF of the CP2₂ the input control voltage V_A should be greater than $2V_T$, where V_T is a threshold voltage of the N channel transistor, N_{b21} or N_{b22} (see Figure 10).

4. Principle of operation

The APWCL is a circuit with nonlinear feedback loop. It controls the duty cycle of the clock signal in complex digital circuits. During this operation, from its start to the steady-state, it passes through the following three different modes of operation:

- *Nonlinear mode* - The voltage difference $V_{ref}-V_c$ is large. The amplifier Amp is saturated and controls voltage $V_{ctrl} \sim 0V$. During this period, see Figure 12, the feedback control loop is out-of-order, but the charge pumps CP1 and CP2 are operative. The response time of CP1 is fast (V_{ref} increases rapidly), while the response time of CP2 is slow (V_c increases linearly and slowly). At the output CLK_{out} , pulses of minimal duty cycle (20%) are generated. Let us note that this is one of the crucial difference compared to solutions proposed by Sung-Rung and Shen-Iuan (2004), and Fenghao and Svensson (2000). Namely, at the output of CLK_{out} , pulses are generated in our proposal during all the time.
- *Linear mode* - when the voltage difference $V_{ref}-V_c$ becomes less than Amp's input threshold V_{lin} the amplifier enters a linear mode of operation. From this moment the linear feedback loop is operative, and corresponding actions concerning corrections of a duty cycle are done.
- *Steady-state mode* – transitions in APWCL operation are stabilized so the duty cycle of CLK_{in} and CLK_{out} is equalized. The voltages V_{ref} , V_c and V_{ctrl} take steady-state values.

4.1. Adaptability

When the Amp is in saturation, the APWCL is in nonlinear mode. If the condition $V_{ref}-V_c \leq \frac{V_{dd}}{A} = V_{lin}$, where $V_{ref}-V_c$ is Amp's input voltage difference is satisfied, A gain of the Amp and V_{dd} is a power supply voltage, then the APWCL operates in a linear mode. Electrical parameters of the charge pump CP2, load

capacitor C_{12} and charge pump current $I_{cp2}=I_{cp}+I_{cp}'$ (see Figure 11), directly determine the time duration, t_{NL} , of the nonlinear APWCL mode of operation, according to the following equation

$$t_{NL} = \frac{C_{12} \cdot V_{c,lin}}{I_{cp2}(1 - 2 \cdot D_{CLKout})} \quad (1)$$

where: D_{CLKout} is duty cycle of CLK_{out} for $V_{ctrl} \sim 0$, and $V_{c,lin}=V_{ref,steady-state} - V_{lin}$ (see Figure 12).

By analyzing eq. (1) we can conclude that: If during the design phase we keep the load capacitor C_{12} fixed and increase I_{cp2} , then we can decrease the time duration of t_{NL} . In a concrete proposal, the current I_{cp} is fixed, while the current I_{cp}' is variable. This possibility allows us to regulate time duration of t_{NL} .

The fixed current I_{cp} is switched ON during all three operating modes, while the variable current I_{cp}' is switched ON in nonlinear mode and switched OFF in linear and steady-state mode. This possibility allows us to decrease drastically the time period t_{NL} . Having in mind that the proposed APWCL architecture, during transition from nonlinear to steady-state, temporally involves, in the feedback loop, additional constituents we say that it is an adaptive one.

In order to achieve adaptability the building block charge pump controller CPC is implemented into APWCL (see Figure 4). It detects the operating mode of APWCL, and according to this, it switches OFF or ON the charge pump CP2₂. The block CP2₂ is part of a charge pump CP2 (see Figure 10).

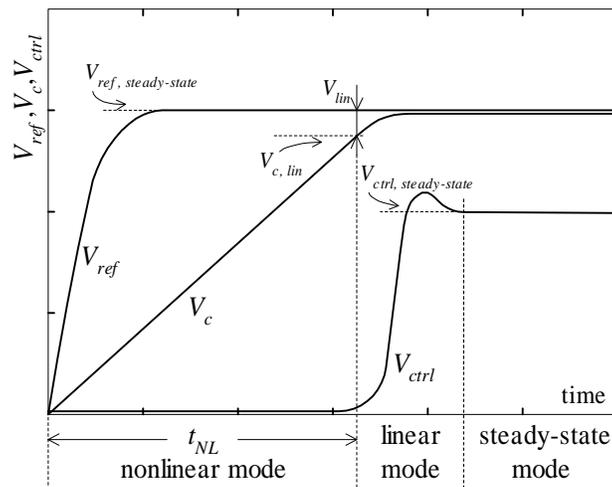


Figure 12. Transient in APWCL

5. On analysis and design of control loop

The structural block scheme of the proposed control loop is shown in Figures 13. As we had seen earlier, the model contains one nonlinear element originated from the amplifier saturation, so we should perform the stability analysis starting with the nonlinear mode of operation first, which is depicted by the Figure 13(a). Since the time delay (clock buffers) is small enough in respect to other time constants in the circuit, it is neglected and considered as non-modelled dynamics.

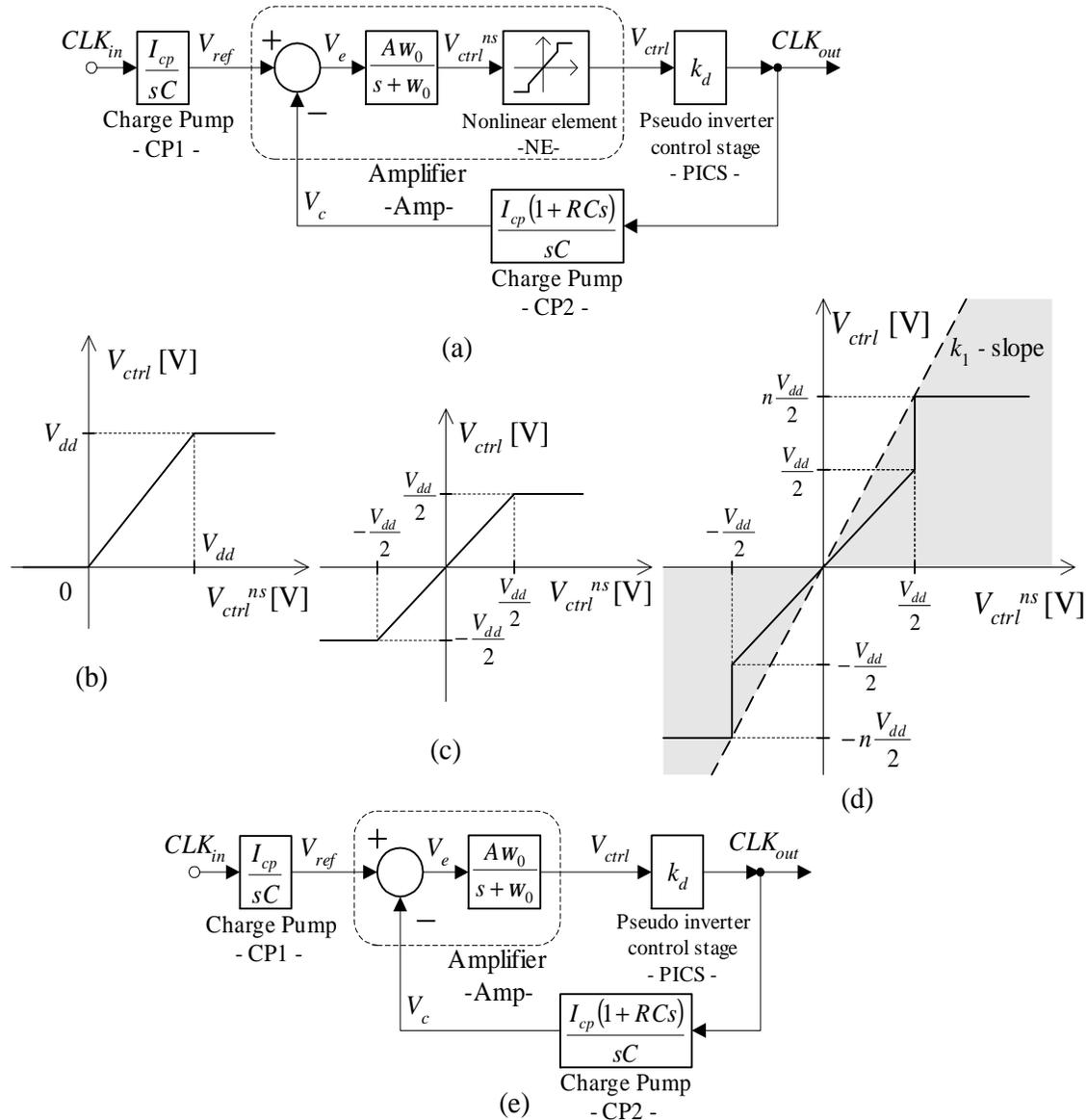


Figure 13. (a) APWCL's structural block scheme for nonlinear mode, (b) Real amplifier saturation characteristic, (c) Amplifier saturation characteristic with omitted dynamics of PICS, (d) Modified (c) characteristic involving adaptive current of CP2, (e) APWCL's structural block scheme for linear mode.

The amplifier saturation can be presented by the non-symmetrical nonlinear characteristic given in Figure 13(b), while the PICS can be modelled by the first-order polynomial according to Figure 8. In our model, these two components are given in different manner, so that the PICS is modelled by the gain block k_d , and the nonlinear element, recognized as a saturation, is rearranged to include the neglected dynamics of the PICS, yielding the symmetrical nonlinear characteristics, presented in Figure 13(c).

In order to evaluate the influence of the adaptive current I_{cp2} of CP2 to the control loop, it can be formulated as $I_{cp2} = I_{cp} + I_{cp}' = nI_{cp}$ where n is a real number. The factor n is now included in the nonlinear element, finally providing the nonlinear element whose characteristic is given in Figure 13(d) and used further for the stability analysis.

5.1. Nonlinear mode

We will now perform the stability analysis in the nonlinear mode, and use the well-known Popov's absolute stability criteria, presented in Appendix A. To implement this criteria to APWCL we concern the following transfer function of the control loop linear part (see Figure 13(a)):

$$G_{OL}(s) = \frac{Aw_0k_dI_{cp}(1+RCs)}{Cs(s+w_0)} \quad (2)$$

and consider its normalized representation:

$$G_{OL}^n(s) = \frac{s+w_1}{s(s+w_0)}, \quad (3)$$

where $w_1 = 1/RC$ and the gain $Aw_0k_dI_{cp}R$ is added to the nonlinear element gain k_1 yielding:

$$k = k_1Aw_0k_dI_{cp}R. \quad (4)$$

By applying $s=jw$ in (3), the normalized frequency response of the system is obtained as:

$$G_{OL}^n(s) = \frac{w_0 - w_1}{w^2 + w_0^2} - j \frac{w^2 + w_0w_1}{w(w^2 + w_0^2)}, \quad (5)$$

and the modified frequency response is accordingly:

$$G_{m-OL}^n(s) = \frac{w_0 - w_1}{w^2 + w_0^2} - j \frac{w^2 + w_0w_1}{w^2 + w_0^2}. \quad (6)$$

We can see that $U_m(0) = \frac{w_0 - w_1}{w_0^2}$ and $V_m(0) = -\frac{w_1}{w_0}$ for $w = 0$, and when $w \rightarrow \infty$, then $U_m(\infty) = 0$ and

$V_m(\infty) = -1$. This means that we can adopt $1/k=0$, as it is presented in Figure 14, and, theoretically speaking,

the gain k and, consequently, the factor n can be arbitrary selected from the interval $[0, \infty)$ to guarantee system absolute stability in the nonlinear mode. The choice of n is then conditioned only by the technology limitations, i.e. by the maximum available current of CP2.

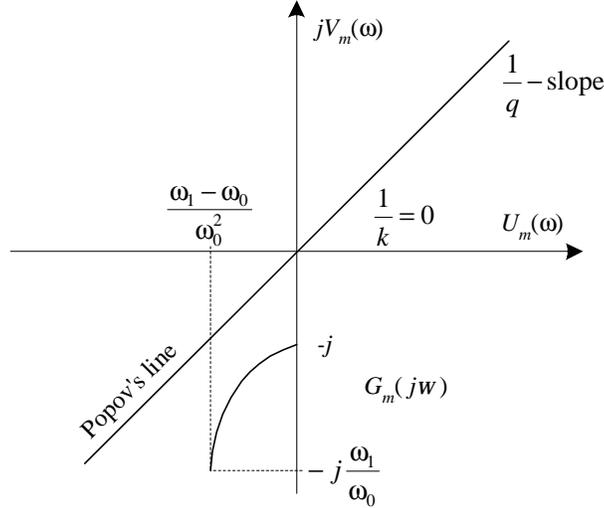


Figure 14. Popov's criteria graphical representation of APWCL.

5.2. Linear mode

When the condition $V_{ref} - V_c \leq \frac{V_{dd}}{A} = V_{lin}$ is satisfied then the APWCL operates in a linear mode. The structural block scheme of the control loop in linear mode is shown in Figures 13(e). The open loop transfer function is identical as the transfer function of linear part of APWCL in nonlinear mode (2):

$$G_{OL}(s) = \frac{V_c(s)}{V_e(s)} = \frac{Aw_0k_dI_{cp}(1+RCs)}{Cs(s+w_0)}. \quad (7)$$

The closed loop transfer function is given by:

$$G_{CL}(s) = \frac{V_c(s)}{V_{ref}(s)} = \frac{\frac{Aw_0k_dI_{cp}}{C}(1+RCs)}{s^2 + (w_0 + Aw_0k_dI_{cp}R)s + \frac{Aw_0k_dI_{cp}}{C}}, \quad (8)$$

and, consequently, the characteristic polynomial is:

$$F_c(s) = s^2 + (w_0 + Aw_0k_dI_{cp}R)s + \frac{Aw_0k_dI_{cp}}{C}. \quad (9)$$

The desired system dynamics in the linear mode is defined by the damping factor α and the nature frequency w_n . The involvement of zero dynamics in CP2 enables an independent choice of α and w_n . These parameters determine the desired characteristic polynomial in the form of:

$$F_c^d(s) = s^2 + 2xw_n s + w_n^2. \quad (10)$$

By comparing the coefficients of (9) and (10), the current I_{cp} of CP2 and the resistor R can be calculated as:

$$I_{cp} = \frac{w_n^2 C}{A w_0 k_d}, \quad (11)$$

$$R = \frac{2xw_n - w_0}{A w_0 k_d I_{cp}}, \quad (12)$$

so that the wanted system dynamics in the linear mode is obtained. It is recommended to select $x=0.707$ to achieve the optimal closed loop response in linear mode.

5.3. Steady-state mode

In order to comment the steady-state APWCL performances, we consider the sensitivity transfer function:

$$S(s) = \frac{V_e(s)}{V_{ref}(s)} = \frac{s(s + w_0)}{s^2 + (w_0 + A w_0 k_d I_{cp} R)s + \frac{A w_0 k_d I_{cp}}{C}}. \quad (13)$$

It is obvious from (13) that the proposed APWCL should have the zero error signal V_e in steady-state when V_{ref} is step signal since $V_e(\infty) = \lim_{s \rightarrow 0} s S(s) V_{ref}(s) = 0$ when $V_{ref}(s) = 1/s$. Unfortunately, there exist the non-zero error in the steady-state due to amplifier input offset and the lack of the symmetry in the design of the charge pumps.

6. APWCL simulation results

SPICE simulation results for APWCL circuit in a $1.2\mu\text{m}$ double-metal double-poly CMOS process with $V_{dd}=5\text{V}$ supply voltage and operating frequency 100MHz , are presented in Figure 15. Comparative, results that relate to the conventional PWCL and proposed APWCL, in Figure 15 (a) and (b), are given respectively. Identical building blocks PICS, CP1, Amp, BC1 are used for both simulations. In both cases, the clock buffer (CB) has 7 stages with tapering factor of 1. Related to conventional PWCL, CP2 is replaced with charge pump whose current is variable in APWCL charge pump. Additional blocks CPC and BC2 are used for current regulation in charge pump CP2.

The circuit's model in linear mode is described by the second order transfer function (8). The desire system's dynamic is defined by choice of the dumping factor x and natural frequency w_n . If the dumping factor is $\xi=0.707$ and natural frequency is $w_n=3 \cdot 10^7 \text{ rad}\cdot\text{s}^{-1}$ according to equation (11) and (12) other

circuits parameters are determined as: $I_{cp1}=I_{cp2}=I_{cp}=10\mu\text{A}$ – corresponds to charge pump current of CP1 and CP2; $A=100$ – DC gain of the Amp; $w_0=2\pi f_0=2\pi 3.5\text{MHz}$ –dominant pole of the Amp; $C_{11}=C_{12}=C=8\text{pF}$ – charge pump capacitor; $R=2800\Omega$ – CP2 load resistance; $k_d=0.32\text{V}^{-1}$ – PICS's sensitivity constant. For nonlinear operating mode $I_{cp2}=I_{cp}+I_{cp}'$ where $I_{cp}'=50\mu\text{A}$.

The waveforms at the top in Figure 15 (a) and (b) correspond to curves of V_{ref} and V_c . The second waveform in Figure 15 (a) corresponds to the control voltage V_{ctrl} . Additionally, in Figure 15 (b), the control voltage V_A , is presented. The two lower waveforms in Figure 15 (a) and (b), depict CLK_{out} pulses valid for nonlinear mode and steady-state mode, respectively.

We start with our simulation from the instant when the system is powered-on ($t=t_0$). This implies that both charge pumps load capacitors, C_{11} and C_{12} , as well as the low-pass filter capacitor C_2 , are discharged. According to the transient response, the following three different modes, in the operation of the feedback loop, can be identified:

a) From t_0 up to t_1 the loop operates in nonlinear mode. Since C_{11} charges faster, in respect to C_{12} , at instant t_0 the voltage V_{ref} becomes greater than V_c and therefore the output of Amp switches rapidly to lower voltage limit, and the control voltage V_{ctrl} is 0V. Under this condition at the CLK_{out} , pulses of minimal pulsewidth are generated. Contrary to the proposals described by Sung-Rung and Shen-Iuan (2004) and Fenghao and Svensson (2000), where in the saturation mode the PWCL is inoperative, i.e. CLK_{out} is blocked, in APWCL pulses of minimal duty cycle, at the output of CLK_{out} , are generated.

b) As the input voltage difference becomes small enough, the amplifier Amp enters linear mode what corresponds to the time interval from t_1 up to t_2 . When the dumping factor $\xi=0.707$, transients in linear mode are minimal.

c) Steady-state operation mode characterizes stable-loop operation and corresponds to the time interval after t_2 . During this period, variations of V_{ctrl} are less than $\pm 25\text{mV}$, i.e. 1.8% in respect to V_{ctrl} (1.5V). As it can be seen from Figure 15, the duty cycle of CLK_{out} in the saturation mode is 20%, and in the steady-state mode it is 51%.

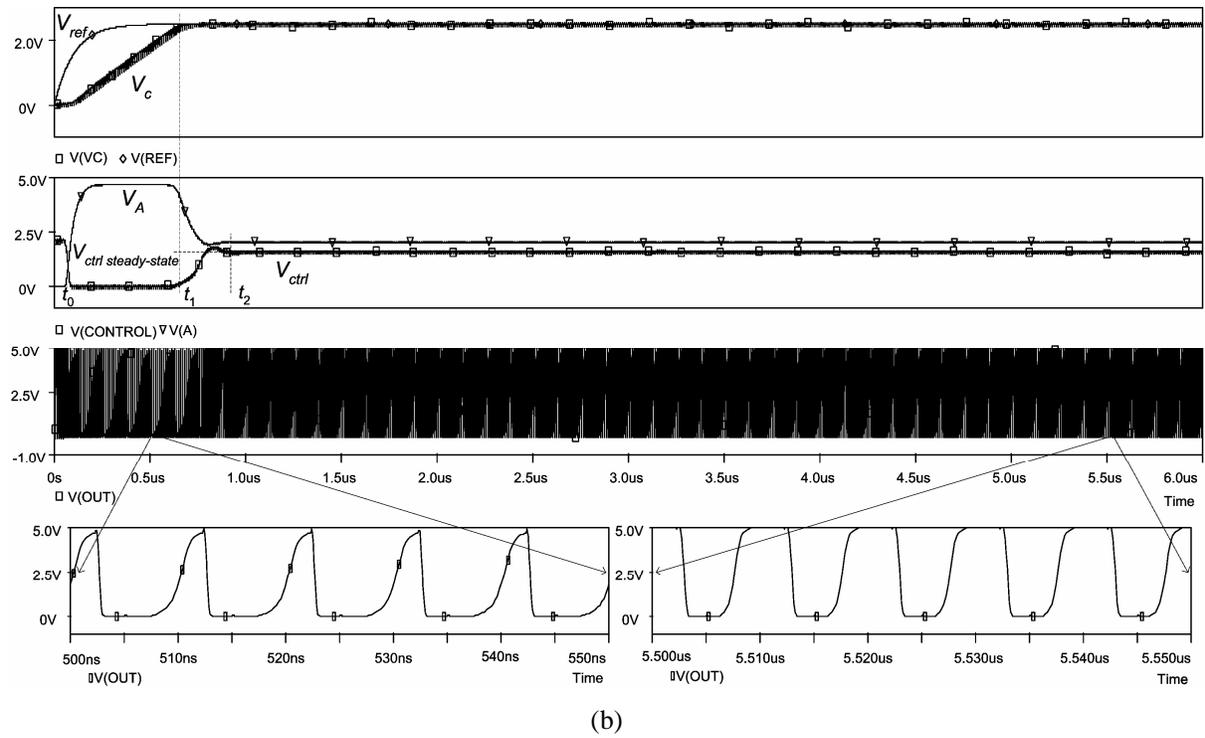
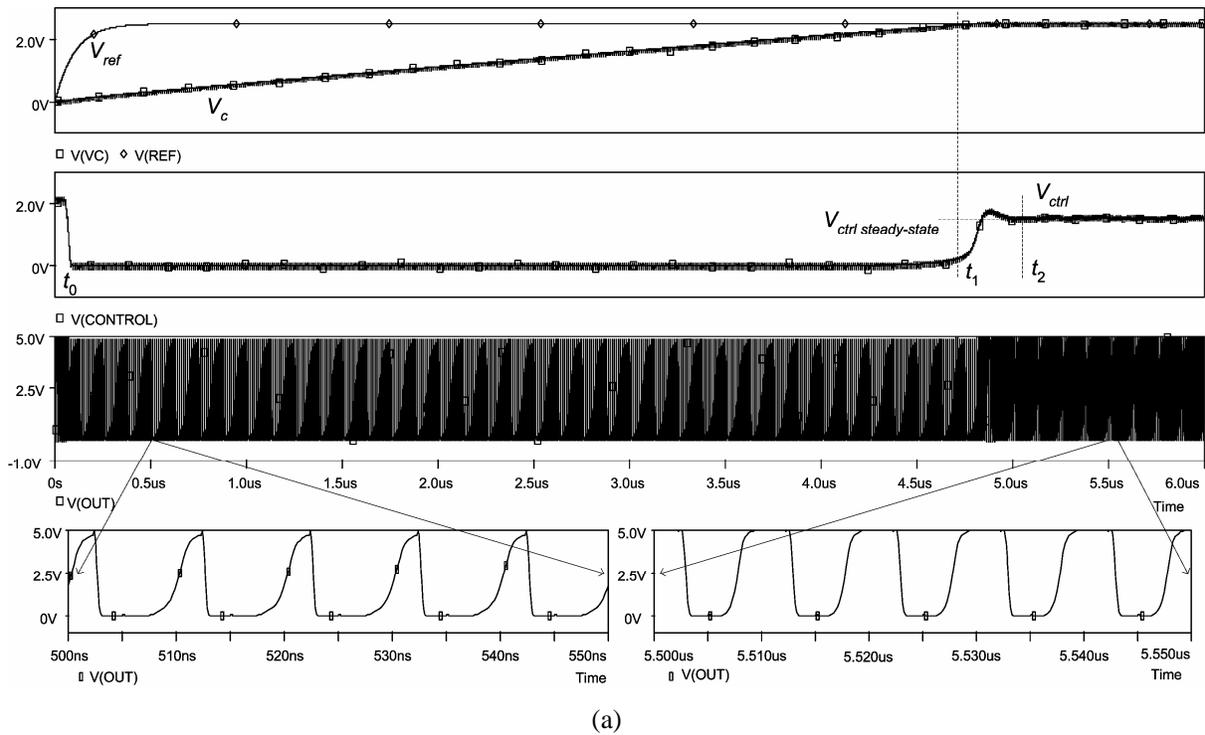


Figure 15. (a) Conventional PWCL and (b) adaptive PWCL simulation results.

The main difference between waveforms in Figure 15 (a) and waveforms in Figure 15 (b) relates to the time duration of nonlinear operating mode, from t_0 up to t_1 . The voltage difference between V_{ref} and V_c during this period is large and the differential amplifier CPC enters in saturation region. The CP2's control voltage V_A is approximately equal to the supply voltage V_{dd} and the current I_{cp} is active. This means that in nonlinear

mode the charge pump CP2 works with current $I_{cp2}=I_{cp}+I_{cp}'=n I_{cp}=60\mu\text{A}$. Increasing CP2's current by a factor n means that the time duration of nonlinear mode t_{NL} is shortened by n , too (see equation (1)). This possibility provides a condition for fast loop locking time.

6. Conclusion

Numerous methods for distributing a clock within a VLSI IC has been discussed in the research literature over the years, such as for example Friedman (2001). The methods vary from the more obvious solution of using asynchronous communication between locally clocked regions as proposed by Johnson and Graham (2003), to more fancy methods like distributing and standing wave on the clock-wire across the whole chip as described by Chi (1994). However, most of today's researches are targeted towards reducing the clock-skew, jitter and symmetrical duty cycle by improving current clock distribution methods. The clock distribution tree within the VLSI ICs is so large and carries so much capacitance that buffers need to be inserted just to be able to drive the clock-tree in order to have a reasonable clock waveform. When the clock passes through a multistage buffer changes its duty cycle. In order to obtain a satisfactory duty cycle correction a fast locking APWCL was proposed. The APWCL adopts almost identical architecture as conventional PWCL described by Fenghao and Svensson (2000) but with two modifications. The first relates to implementation of the pseudo inverter control stage (PICS), which is operative during all APWCL's mode of operation. This possibility provides pulses generation at the output of APWCL during all mode of operation. The second modification represents involvement of adaptive control loop, which provides shorter transient time of the nonlinear mode, i.e. faster locking time. SPICE simulation results, for 1.2 μm double-metal double-poly CMOS process with $V_{dd}=5\text{V}$ and 100MHz operating frequency, show that the duty cycle can be controlled in the range from 20% up to 80%.

Appendix A

Theorem 1 (Popov 1961): A nonlinear control system with linear part whose frequency response is $G(j\omega)$

and a nonlinearity satisfying $0 \leq \frac{F(e)}{e} \leq k$ (Figure A1), if $G(j\omega)$ has only stable poles, or $0 < \frac{F(e)}{e} \leq k$,

when $G(j\omega)$ has all stable poles except one in the origin, is said to be stable if there exist a real number q so that the inequality:

$$\operatorname{Re}\{(1 + jq\omega)G(j\omega)\} + \frac{1}{k} \geq 0 \quad (\text{A1})$$

is valid for every $\omega \geq 0$.

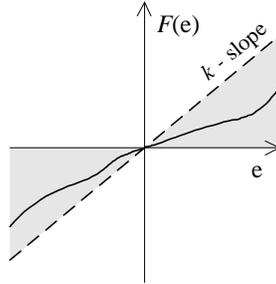


Figure A1. Nonlinear characteristic.

Denoting $G(j\omega) = U(\omega) + jV(\omega)$, (A1) becomes:

$$U(\omega) + j\omega V(\omega) + \frac{1}{k} \geq 0. \quad (\text{A2})$$

The inequality (A2) has its graphical representation, illustrated in Figure A2 and explained as follows.

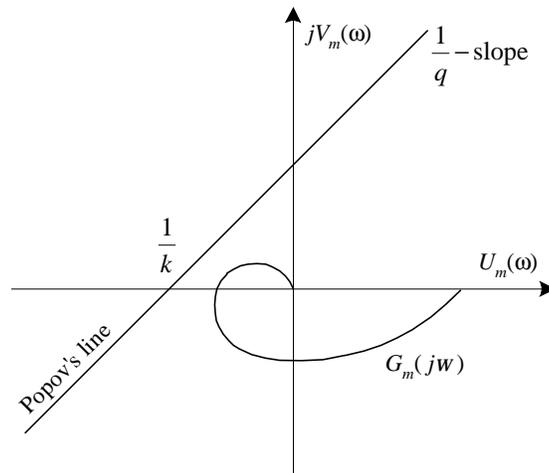


Figure A2. Popov's criteria graphical representation.

Theorem 2: A nonlinear control system with linear part whose frequency response is $G(j\omega)$ and a nonlinearity satisfying $0 < \frac{F(e)}{e} < k$ is absolute stable if a modified frequency response of system linear part, defined as

$$G_m(j\omega) = U_m(\omega) + jV_m(\omega) = U(\omega) + j\omega V(\omega), \quad (\text{A3})$$

is always on the right side from the so-called Popov's line determined as:

$$V_m(\omega) = \frac{1}{q}U_m(\omega) + \frac{1}{qk}. \quad (\text{A4})$$

for $w \in [0, \infty)$.

When $G(jw)$ has one pole in the origin, Popov's criteria should be integrated with condition:

$$\lim_{w \rightarrow 0} V(w) = \infty \quad (\text{A5})$$

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