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Clock aligner based on delay locked loop with double edge synchronization

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Abstract

In CMOS multistage clock buffer design, the duty-cycle of clock is liable to be changed when the clock passes through several buffer stages. The pulse-width may be changed due to unbalance of the p- and n-OS transistors in the long buffer. This paper describes a delay locked loop with double edge synchronization for use in a clock alignment process. Results of its SPICE simulation, that relate to 1.2 μm CMOS technology, shown that the duty-cycle of the multistage output pulses can be precisely adjusted to $(50 \pm 1)\%$ within the operating frequency range, from 55 MHz up to 166 MHz.

1. Introduction

Almost all contemporary digital VLSI systems and other digital systems rely on clock pulses to control the movement of data. To reach the highest circuit speed in CMOS applications, the clock distribution system must be carefully designed. A great deal of attention has been paid to clock recovery, clock regeneration, timing, and distribution during the last several years [1–3]. In [4], numerous clocking techniques and hardware structures of clocked storage elements for high-performance and low-power system are discussed.

Automatic control techniques, such as phase-locked loop (PLL) and delay-locked loop (DLL) have been widely used in high-speed clock alignment applications such as double-data rate (DDR) SDRAMs, pipelined microprocessors, network processors, etc. [5,6].

In a PLL implementation the chip has its own reference clock oscillator (VCO) that is phase-locked to an external reference clock. In general, a PLL clock aligner is superior in applications where noise on the reference clock dominates, and self-induced jitter within the VCO is negligible. On the other hand, a DLL provides superior performance when a clean reference clock is available. A DLL is commonly used to lock the phase of the buffered clock to that of the input data. Typically, we meet this in applications where no clock synthesis is required, such as often the situation for multi-chip digital systems with well-designed system clock distribution network [5].

In high-speed design a multistage clock buffer implemented with a long inverter chain is often needed to drive a heavy capacitive load. For these designs, as well as for applications in which the timing of both edges of the clock is critical [7], it is difficult to keep the clock duty cycle at its ideal value 50%, primarily due to various asymmetries in signal paths and unbalances of the p and n transistors in the long buffer. As a consequence the clock duty cycle will deteriorate from 50%, and in the worst case, the clock pulse may disappear inside the clock buffer, as the pulse width becomes too narrow or too wide [8]. In Ref. [9], several structures of storage elements, that allow the same data throughput with half of the clock frequency, referred to as double-edge triggered clocked storage elements (DETSE) are described. In addition, a comparison of DETSE with their single-edge triggered counterparts in

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terms of delay and power consumption is given. A classification, detailed timing characterization, evaluation, and design of the DETSE is presented in [10]. For more details related to results of experiments with dual-edge clocking processor for low-power see [11].

Duty-cycle distortion is usually addressed in PLLs by simply running the PLL's VCO at twice the system frequency and using a post-divider triggered on one edge of the VCO output to produce the output clock of the PLL. This ensures good 50% duty cycle. In a DLL, however no frequency multiplication is possible. Therefore, the duty-cycle of the output signal must be corrected to 50%. A conventional solution is to attach duty-cycle correction circuit to the clock output driver with the price of added area [12].

In this paper, we describe a new structure of a DLL circuit with clock alignment capability of both leading and trailing output pulse edges. This circuit can be used to obtain correct the duty-cycle factor (50%) in a multistage clock buffer. The rest of the paper is organized as follows. In Section 2 general structures of clock aligner circuits based on DLL and PLL approaches are depicted. In Section 3 the architecture, principle of operation and corresponding mathematical model of a delay locked loop with double edge synchronization, called DLL-DES, are described. Section 4 concentrates on implementation of DLL-DES's constituents. Results obtained by SPICE simulation are presented in Section 5. Conclusions are given in Section 6.

2. Clock aligners

The goal of the clock distribution network is to organize clocking so that the delays from the source point of each clock or clock phase to its destination points are identical. In reality, however, no matter how each clock path is constructed, due to variations in wire delays and driver delays, no-uniform and possibly time-varying clock load, and negative effects of supply and substrate noise, any two paths within the VLSI IC will always have a delay difference. A clock aligner's task is to phase-align a chip internal clock with a reference clock, effectively removing the variable buffer delay and reducing uncertainty in clock phase between communicating VLSI IC constituents. Clock aligners (see Fig. 1) can be built using either PLLs or DLLs.

In a PLL implementation (Fig. 1a) the circuit has its own oscillator (voltage controlled oscillator – VCO) that is phase-locked to a reference clock, CLK_{ref}. The phase shift introduced by the clock buffers' delay, T_B, is assumed to be changing as a consequence of wiring delay, temperature and voltage variations, etc. The clock buffers' delay is eliminated by its inclusion in the control loop.

In DLL implementation (Fig. 1b) a voltage controlled variable delay line (VCDL) is inserted between the reference clock, CLK_{ref}, and the output clock, CLK_{out}. The delay is regulated so that $T_D + T_B = N \times T_{ref}$ (usually $N = 1$), where T_D and T_B relate to pulse time propagation through VCDL and Clock Buffer, respectively, and T_{ref} corresponds to referent clock pulse period. The clock buffers' delay is placed within a control loop and is eliminated.

PLL and DLL implementations have complementary advantages and disadvantages. Table 1 summarizes the main features of PLL and DLL clock aligners.

Many factors control the speed of CMOS ICs, such as device dimensions, clocking strategy, architecture, clock distribution, etc. Here we focus our attention on clocking strategy and clock distribution problems.

To meet the demand for high-speed operation today, many systems adopt a double data rate (DDR) technologies, such as DDR SDRAM, double sampling ADC, clock and data recovery circuits, microprocessor circuits, etc. In these systems, both rising and falling edges of the clock are used to sample the input data, requiring that the duty-cycle of the clock be precisely maintained at 50%. Therefore, how to generate a clock with precise 50% duty-cycle for high-speed operation is an important issue. Namely, in high-frequency operations, clock outputs with a short cycle time can be severely distorted as clock passes through many delay cells. Even if the duty cycle of CLK_{ref} is 50% at the entrance, that of CLK_{out} may deviate significantly from 50%. As a consequence, it can cause

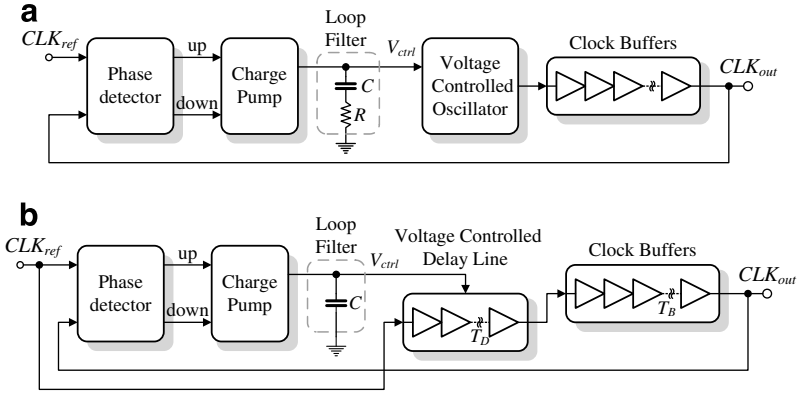

Fig. 1. Clock aligner implementations: (a) PLL clock aligner and (b) DLL clock aligner.

Table 1
Comparisons of PLL and DLL

PLL	DLL
Jitter accumulation	No jitter accumulation
Higher-order system	1st-order system
Can be unstable	Always stable
Hard to design	Easier to design
Costly to integrate loop filter	Easier to integrate loop filter
Less referent signal dependent	Referent signal dependent
Easy frequency multiplication	Difficult frequency multiplication
additional hardware is not needed	Additional hardware is needed
Wide locking range	Limited locking range

the output to have phase error, which could be fatal, especially in high-speed communication applications.

A conventional solution is to attach duty-cycle correction circuits to all output drivers with the price of added area, increased jitter, and further phase mismatch due to enlarged path [12]. There are several different methods for implementing 50% duty-cycle correctors, both in PLL and DLL control loops, intended to adjust the output duty-cycle of the multistage driver [8,13–15]. Some of these methods are analog [16], while others are digital [17]. Each of these methods has its advantages and drawbacks. In all these circuits, the variable delay element is one of the key building blocks. Its precision directly affects the overall performance of the circuit.

3. DLL with double edge synchronization

The structure of the proposed delay locked loop with double edge synchronization (DLL-DES) clock alignment circuit is pictured in Fig. 2. The clock aligner is composed of a voltage controlled delay line, VCDL, two phase detectors, PD1 and PD2, two charge-pumps, CP1 and CP2, two first order low-pass filters, LP1 and LP2, and a multistage clock buffer, CB. The negative feedback in the loop adjusts the delay through the VCDL by integrating the phase shift errors that result between the periodic reference input, CLK_{ref}, and the multistage output, CLK_{out}.

The underlying idea for this approach is to provide delay regulation for both a rising and trailing edge of the output clock pulse CLK_{out}. For implementation of variable delay regulation the building block VCDL is used. The control voltage V_{bn} (V_{bp}) defines delay regulation of a rising (trailing) clock pulse edge. The phase detector PD1 (PD2) compares a phase shift of rising (trailing) edges between the input, CLK_{in}, and output, CLK_{out}, clock pulses. UP1 (UP2) pulses cause I_p to add charge to loop filter capacitor C, whereas DN1 (DN2) pulses remove charge. The LP1's (LP2's) output, V_{ctrl1} (V_{ctrl2}), is connected to the VCDL control input at node V_{bn} (V_{bp}). When the system, from Fig. 2, enters in stable state both edges of CLK_{out} are synchronized and phase shifted in respect to the referent clock CLK_{ref}. An important feature of this architecture is that the duty-cycle of CLK_{out} is maintained at value of 50%.

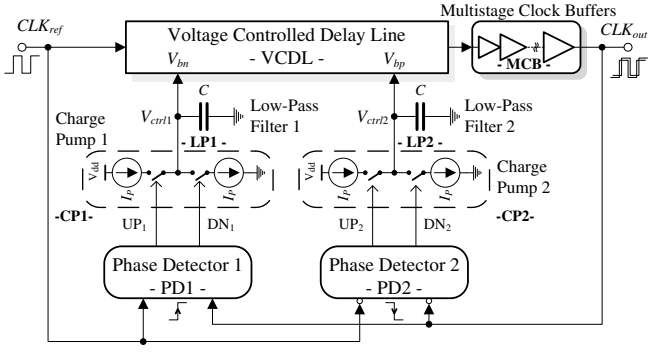

Fig. 2. DLL's architecture with double edges synchronization.

3.1. Equivalent model of DLL-DES: transfer function and pulse-width

The equivalent model of a DLL-DES is pictured in Fig. 3. It is decomposed into two independent control loops, DLL-R and DLL-F. The upper one, DLL-R, determines a time delay of the output rising edge, while the lower, DLL-F, define the time delay of falling edge. Both control loops are of almost identical structure. The differences are the following:

(i) The phase detector PD1 is sensitive to a rising, while PD2 to a falling pulse edge;
(ii) The voltage controlled delay line VCDL-R defines the time delay of a rising output pulse edge, while VCDL-F of the falling edge.

The building block CP1 has identical transfer function as CP2. The transfer functions of constituents LP1 and LP2 are identical, too.

Having in mind that the delay alignment is performed independently for the rising and falling edge, in the analysis that follows, we assume that DLL-DES's operation can be described as independent activities of two separate loops. Our analysis is based on frequency response of the DLL and is similar to that one described in [18]. Accordingly, for the upper loop, the output pulse delay $D_{outR}(s)$, is related to the input delay, $D_{refR}(s)$, by

$$D_{outR}(s) = (D_{refR}(s) - D_{outR}(s)) \cdot k_{PDR} \cdot k_{CPR} \cdot k_{LPR} \cdot k_{DLR} \tag{1}$$

where

$$k_{PDR} = \frac{dDC_{PDR}}{dD} = \frac{1}{T_{ref}} \quad \text{corresponds to phase detector sensitivity}$$

$$k_{CPR} = \frac{dI_{CPR}}{dDC_{PDR}} = I_{CPR} \quad \text{charge pump current sensitivity}$$

$$k_{LPR} = \frac{dV_{ctrl1}}{dI_{CPR}} = \frac{1}{sC_R} \quad \text{loop filter transfer function and}$$

$$k_{DLR} = \frac{dD}{dV_{ctrl1}} \quad \text{delay line sensitivity,}$$

with f_{ref} – frequency of the referent clock, CLK_{ref}; T_{ref} – time period of referent clock; DC – duty-cycle of PD1's

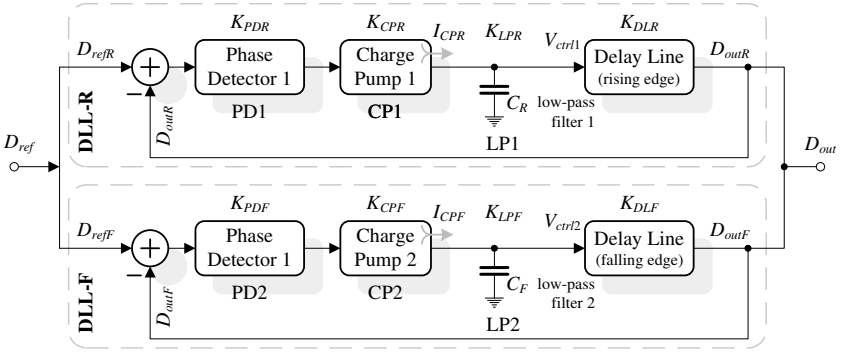

Fig. 3. Equivalent model of DLL-DES.

output at f_{ref}; $D = D_{\text{out}R} - D_{\text{ref}R}$ – delay difference; I_{CPR} – output charge pump current; and C_R –filter capacitance.

By rearranging Eq. (1), for the DLL's closed loop transfer function, $H_{\text{DLL}R}(s)$, we obtain

$$H_{\text{DLL}R}(s) = \frac{D_{\text{out}R}(s)}{D_{\text{ref}R}(s)} = \frac{k_{\text{PD}R} \cdot \frac{k_{\text{CP}R}}{sC_R} \cdot k_{\text{DL}R}}{1 + k_{\text{PD}R} \cdot \frac{k_{\text{CP}R}}{sC_R} \cdot k_{\text{DL}R}} = \frac{1}{1 + s \cdot \frac{C_R}{k_{\text{PD}R} \cdot k_{\text{CP}R} \cdot k_{\text{DL}R}}} = \frac{1}{1 + \frac{s}{\omega_{NR}}} \tag{2}$$

where $\omega_{NR} = \frac{k_{\text{PD}R} \cdot k_{\text{CP}R} \cdot k_{\text{DL}R}}{C_R} = \frac{f_{\text{ref}} \cdot I_{\text{CP}R} \cdot k_{\text{DL}R}}{C_R}$ represents a pole of the DLL's transfer function.

By analyzing Eq. (2) we conclude that the DLL has first order transfer function and the frequency of its pole corresponds to a loop bandwidth.

The delay at the DLL-DES's output can be determined according to the transfer function which is obtained using an identical approach as one for conventional DLL architecture. Concerning the rise pulse edge, a transfer function has the form defined by Eq. (2). Accordingly the delay of a rising edge is defined by

$$D_{\text{out}R}(s) = H_{\text{DLL}R}(s) \cdot D_{\text{in}R}(s) = \frac{1}{1 + \frac{s}{\omega_{NR}}} \cdot D_{\text{in}R}(s). \tag{3}$$

For the transfer function of the falling edge, $H_{\text{DLL}F}(s)$, we have

$$H_{\text{DLL}F}(s) = \frac{D_{\text{out}F}(s)}{D_{\text{in}F}(s)} = \frac{1}{1 + \frac{s}{\omega_{NF}}} \tag{4}$$

where $\omega_{NF} = \frac{f_{\text{ref}} \cdot I_{\text{CP}F} \cdot k_{\text{DL}F}}{C_F}$.

The delay of a falling edge is

$$D_{\text{out}F}(s) = H_{\text{DLL}F}(s) \cdot D_{\text{in}F}(s) = \frac{1}{1 + \frac{s}{\omega_{NF}}} \cdot D_{\text{in}F}(s). \tag{5}$$

The pulse-width W_{ref} and W_{out} of the reference clock, CLK_{ref}, and from the DLL-DES's output, CLK_{out} (see Fig. 2) are defined as $W_{\text{ref}} = D_{\text{in}R} - D_{\text{in}F}$ and $W_{\text{out}} = D_{\text{out}R} - D_{\text{out}F}$, respectively.

The pulse-width of the DLL-DES's output depends on a difference between $D_{\text{out}R}$ and $D_{\text{out}F}$ and is defined as

$$W_{\text{out}}(s) = D_{\text{out}R}(s) - D_{\text{out}F}(s) = \frac{1}{1 + \frac{s}{\omega_{NR}}} \cdot D_{\text{in}R}(s) - \frac{1}{1 + \frac{s}{\omega_{NF}}} \cdot D_{\text{in}F}(s) \tag{6}$$

Due to symmetry in the DLL-DES, i.e. identical realizations of the upper and lower branch in the circuit model presented in Fig. 3, the following is valid, $\omega_{NR} = \omega_N = \omega_N$. Accordingly, Eq. (6) can be written as

$$W_{\text{out}}(s) = \frac{1}{1 + \frac{s}{\omega_N}} \cdot (D_{\text{in}R}(s) - D_{\text{in}F}(s)) = \frac{1}{1 + \frac{s}{\omega_N}} \cdot W_{\text{ref}}(s) \tag{7}$$

Finally, the transfer function $H_W(s)$ which defines the ratio between the output and input pulse-width is given as

$$H_W(s) = \frac{W_{\text{out}}(s)}{W_{\text{ref}}(s)} = \frac{1}{1 + \frac{s}{\omega_N}} \tag{8}$$

By analyzing Eq. (8) we can conclude that the DLL-DES is:

- first order system,
- always stable, and
- the duty-cycle of the referent input, CLK_{ref}, and output pulse, CLK_{out}, is identical, an is equal to 50%.

4. Circuits implementation

In the sequel we will describe, in more details, the structure and principle of operation of each constituent of the DLL-DES based clock aligner.

4.1. Voltage controlled delay line

The actual implementation of a VCDL consists of a chain of variable delay buffers. Each delay buffer (adjustable timing element) is of identical structure. Current starved delay element (CSDE) was chosen as a convenient candidate for realization of the delay buffer. The main design decision for such a choice was the following: CSDE

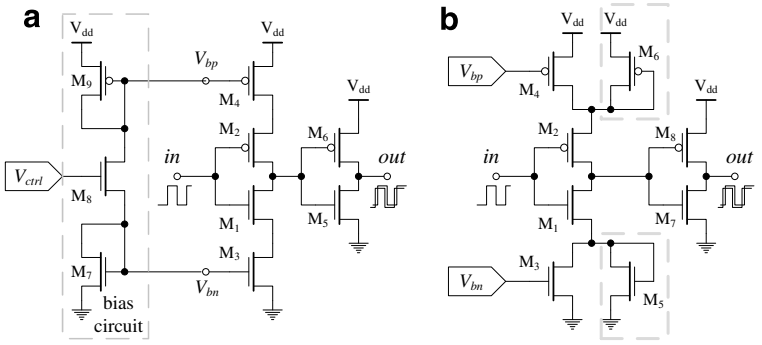

Fig. 4. Modified current starved delay element.

provides independent delay regulation of both rising and falling clock pulse edges. Independent delay regulation can be achieved by varying the current of the p and n-MOS transistors.

In conventional CSDE (see Fig. 4a) a single control voltage V_{ctrl}, generated by a bias circuit, modulates the on resistance of pull-down M_3, and through a current mirror, pull-up M_4 [19]. The variable resistances control the current available to charge or discharge the parasitic load capacitance.

In order to achieve independent, instead of single, variable resistances control, we propose here a modified version of CSDE, as one given in Fig. 4b. In our approach, both control voltages, V_{bn} and V_{bp}, directly drive gates of M_3 and M_4 MOS transistors, respectively. Transistors M_5 and M_6 act as symmetric loads and are used for two purposes: (a) to make linear a voltage-to-delay transfer function of the CSDE; and (b) provides correct initial condition for DLL operation even in a case when both control voltages V_{bn} and V_{bp} are out-of-regulation limits (for example, M_3 and M_4 are switched off).

The delay element is realized as two-inverter stage. The propagation delay of the first stage, t_1, depends on gate voltages V_{bn} (defines the delay of a falling edge t_{1F}) and V_{bp} (defines the delay of a rising edge t_{1R}) [20], respectively, that are defined as

$$t_{1F} = \frac{\tau}{\sqrt{\frac{k_3}{k_5}}(V_{\text{bn}} - V_{\text{tn}})} \times \arctan \frac{\frac{V_{\text{dd}}}{2} \cdot \sqrt{\frac{k_3}{k_5}}(V_{\text{bn}} - V_{\text{tn}})}{\frac{k_3}{k_5}(V_{\text{bn}} - V_{\text{tn}})^2 + \left(\frac{V_{\text{dd}}}{2} - V_{\text{tn}}\right) \cdot (V_{\text{dd}} - V_{\text{tn}})} \tag{9}$$

$$t_{1R} = \frac{\tau}{\sqrt{\frac{k_4}{k_6}}(V_{\text{dd}} - |V_{\text{tp}}| - V_{\text{bp}})} \times \arctan \frac{\frac{V_{\text{dd}}}{2} \cdot \sqrt{\frac{k_4}{k_6}}(V_{\text{dd}} - |V_{\text{tp}}| - V_{\text{bp}})}{\frac{k_4}{k_6}(V_{\text{dd}} - |V_{\text{tp}}| - V_{\text{bp}})^2 + \left(\frac{V_{\text{dd}}}{2} - |V_{\text{tp}}|\right) \cdot (V_{\text{dd}} - |V_{\text{tp}}|)} \tag{10}$$

where k_3, k_4, k_5 and k_6 are constants determined by technology parameters and transistor geometry; V_{tn} and V_{tp} – threshold voltages; and V_{dd} – supply voltage.

The pulse propagation time, t_2, of a second stage is fixed (i.e. does not depend of the control voltage) and is defined by [21]:

$$t_{2F} = \frac{C_{L2}}{k_7(V_{\text{dd}} - V_{\text{tn}})}\left[\frac{2 \cdot V_{\text{tn}}}{V_{\text{dd}} - V_{\text{tn}}} + \ln\left(\frac{4 \cdot (V_{\text{dd}} - V_{\text{tn}})}{V_{\text{dd}}} - 1\right)\right] \tag{11}$$

$$t_{2R} = \frac{C_{L2}}{k_8(V_{\text{dd}} - |V_{\text{tp}}|)}\left[\frac{2|V_{\text{tp}}|}{V_{\text{dd}} - V_{\text{tn}}} + \ln\left(\frac{4(V_{\text{dd}} - |V_{\text{tp}}|)}{V_{\text{dd}}} - 1\right)\right] \tag{12}$$

where C_{L2} – output load capacitance of the second stage; V_{dd} – supply voltage; k_7 and k_8 – technology parameter; and V_{tn}, V_{tp} – threshold voltages.

The total time delay, D, of the current starved delay element pictured in Fig. 4b is obtained by summing pulse propagation delays through both inverter stages, i.e. $D = t_1 + t_2$. The delay of a rising, D_R, and falling edge, D_F, respectively, is defined as:

$$\begin{aligned} D_R &= t_{1F} + t_{2R} \\ D_F &= t_{1R} + t_{2F} \end{aligned} \tag{13}$$

The modified CSDE was designed for 1.2 μm CMOS technology, and for 5 supply voltage. A SPICE simulation results that correspond to delay functions of both rising and falling pulse edges are sketched with full-filed lines in Fig. 5, while those that correspond to the analytical models defined by Eqs. (9)–(13) are pictured with dashed line. The

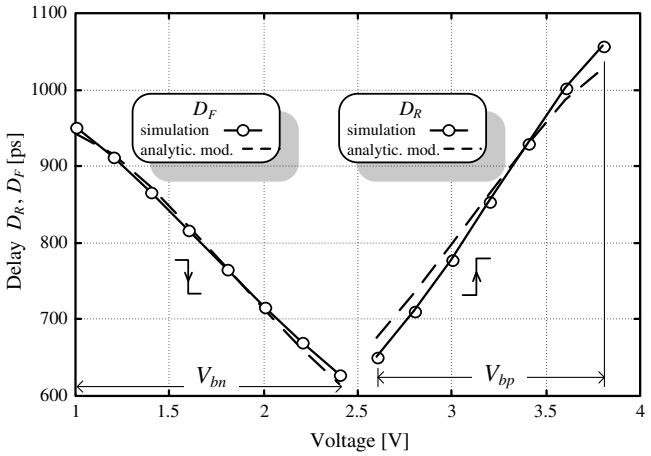

Fig. 5. Rising and falling edge delay in term of control voltages.

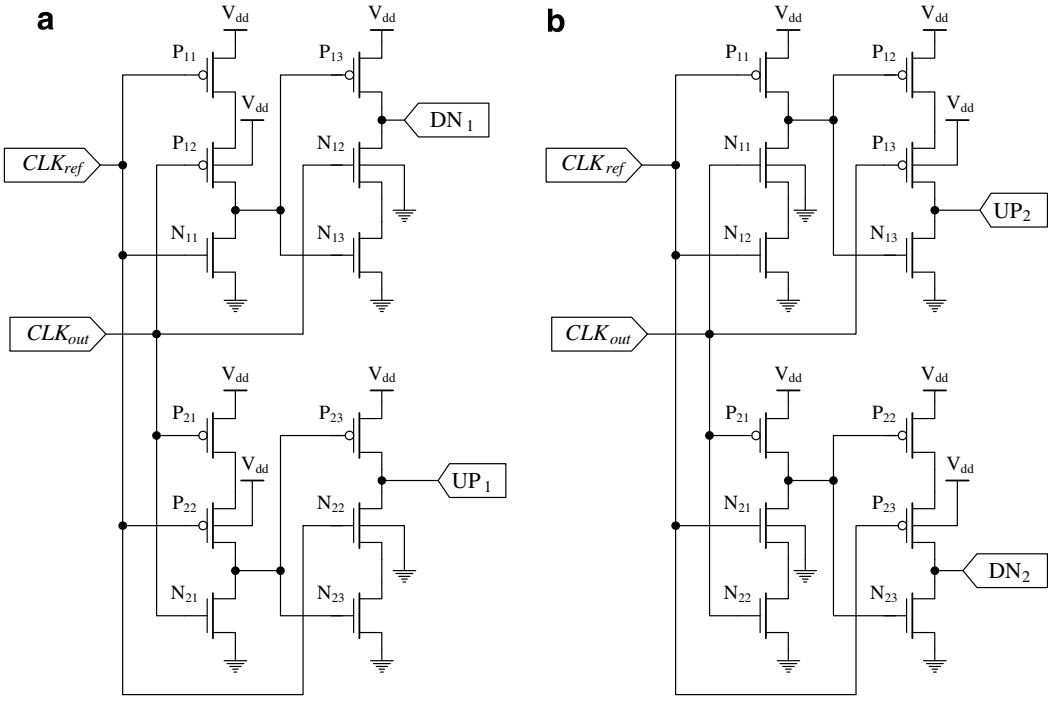

Fig. 6. Implementation of phase detectors for (a) raising and (b) falling edges.

obtained results (see Fig. 5) show that linear regulation of voltage-versus-delay can be achieved. In addition, good agreement (<5%) between the analytical model and results of simulation exists [20]. In general, CSDE offers good delay stability in respect to temperature and supply voltage variations. Its main disadvantage is relatively limited range of delay regulation.

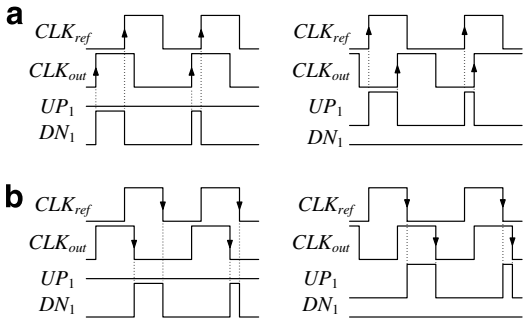

Fig. 7. Waveforms of input and output signals for (a) phase detector 1 and (b) phase detector 2.

The nominal delay which corresponds to one clock time period determines the optimal number of delay elements in the chain. Let note that our delay element (Fig. 4) is designed as non-inverting stage, so in general, an arbitrary number of delay elements can be build in the structure of the VCDL from Fig. 2. The VCDL from Fig. 2 was implemented as a chain of twelve delay elements. Let note that according to SPICE simulation, the delay sensitivity for the rising edge was $k_{\mathrm{DL}R} = \mathrm{d}D_R/\mathrm{d}V_{\mathrm{bn}} = -2.76$ ns/V, and that for the falling edge was $k_{\mathrm{DL}F} = \mathrm{d}D_F/\mathrm{d}V_{\mathrm{bp}} = 4.06$ ns/V.

4.2. Phase detector

The phase detector measures the phase difference between the time reference and the delay chain. High precision dynamic phase detection circuit based on true single

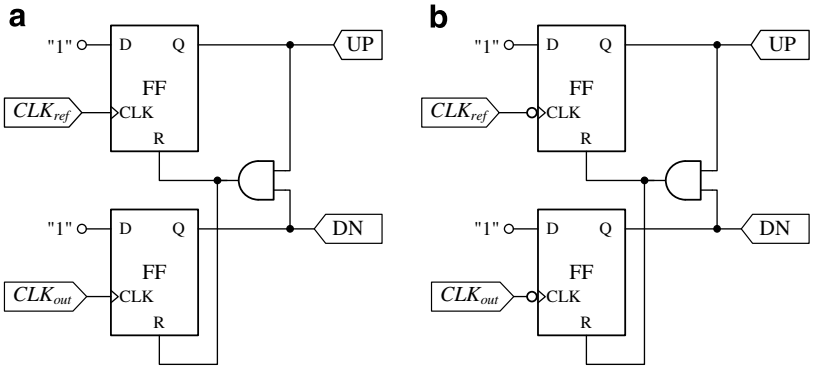

Fig. 8. Equivalent logical model of phase detectors for (a) raising and (b) falling edges.

phase logic [22] is adopted in our design. The main advantages of this circuit are simple hardware structure, high-speed of operation, and small dead zone [19,23]. The UPx and DNx (x refers to 1 or 2) are used to control the charge-pump circuit CPx. The PD1 (PD2) is sensitive to rising (falling) clock pulse edge. A modification, in respect to standard solution [19], is performed by substituting MOS transistors P_{12}, N_{12}, P_{22}, and N_{22} (see Fig. 6a) with complementary ones N_{11}, P_{13}, N_{21}, and P_{23} (see Fig. 6b, respectively.

Operational principles of PD1 and PD2 are shown in Fig. 7. The widths of UP and DN signals are proportional to the phase difference of the input signals. Fig. 7a (b) shows the operation of PD1 (PD2). Waveforms on the left side of Fig. 7a (b) correspond to a case when the signal CLK_{out} (see Fig. 2) leads in respect to the signal CLK_{ref}. Otherwise, timing diagrams on the right side are valid (CLK_{ref} leads the CLK_{out} signal).

The phase detector is in essence a digital circuit sensitive to rising/falling edge. In our proposal, the circuits sketched

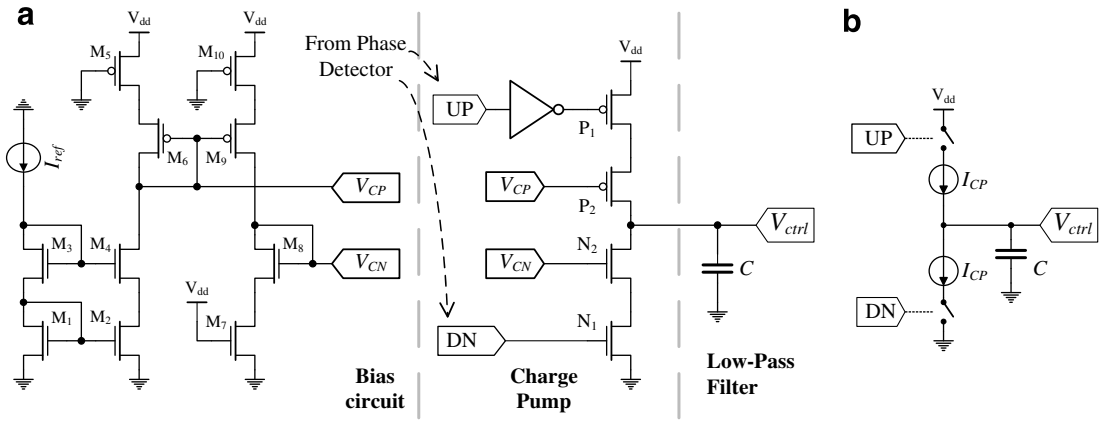

Fig. 9. Current charge pump and loop filter implementation (a) and model (b).

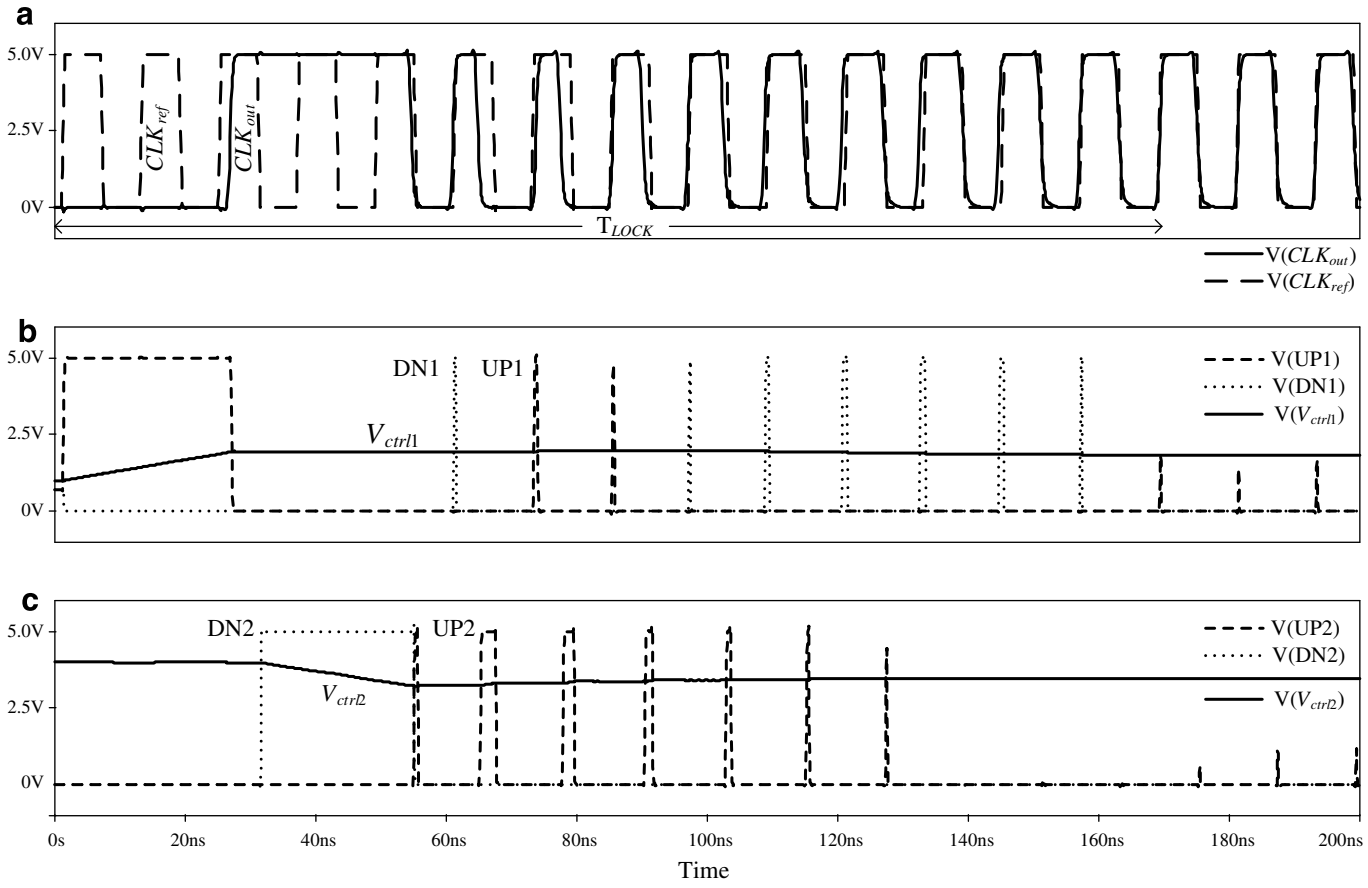

Fig. 10. Simulation of DLL with double edges synchronization.

in Fig. 6 are represented with their equivalent circuits as is given in Fig. 8. Both detectors, for rising and falling edge, are implemented with two D-flip flops, synchronously set by CLK_{in} and CLK_{out} pulses, and asynchronously reset through an AND gate. Reset input, R, is active when both UP and DN outputs are high.

4.3. Charge pump and loop filter

The charge-pump and loop filter structure is presented in Fig. 9a. Transistors P_1 and N_1 act as switching elements driven by pulses UP and DN, while transistors P_2 and N_2 are employed as current sink and source, respectively. The charge-pump charges or discharges the filter capacitor, C. The voltage on this capacitor, V_{ctrl} (V_{bp} or V_{bn} in Fig. 2), sets the VCDL stage propagation delay. The charge-pump the realization of an integrator transfer function with no additional active amplifier, resulting in a zero-phase error in steady state. A small capacitor, C, is used for the low-pass loop filter. The current level of the charge-pump and the charge delivered/accepted at every rising/falling clock edge transition are set to a small value [19]. This allows the implementation of the loop capacitor on chip.

The bias circuit provides correct operation of the charge pump. Its structure is given on the left side of Fig. 9a. This circuit generates two control voltages, V_{CP} and V_{CN}. These voltages define the charge and discharge currents of loop capacitor, C, that pass through transistors P_2 and N_2.

An equivalent model of the circuit from Fig. 9a is presented in Fig. 9b. The circuit is characterized by entire symmetry, i.e. its upper and lower branches are electrically equivalent. We assume that UP and DN switches are ideal. Source and sink currents are equal and adjusted to be $I_{CP} = I_{CPR} = I_{CPF} = 100\ \mu A$. Low-pass filter capacitors for both upper and lower branches are identical too, and are adjusted to $C = C_R = C_F = 2$ pF.

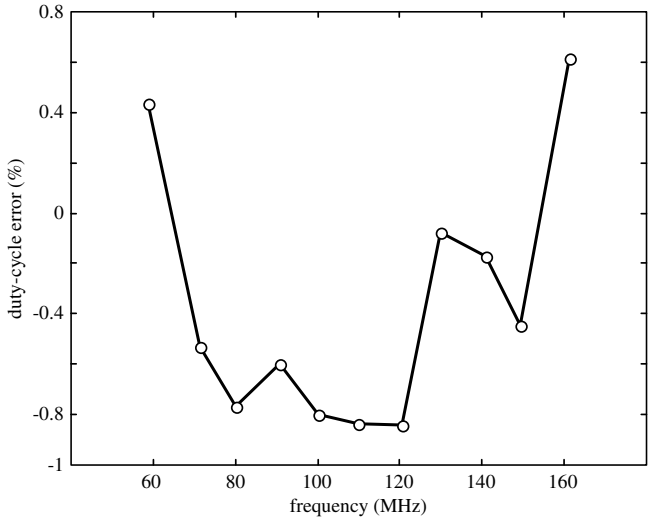

Fig. 11. Duty-cycle error.

5. Simulation results

The DES-DLL sketched in Fig. 2 is implemented in 1.2 μm CMOS technology. It is supplied with $V_{dd} = 5$ V. SPICE simulation results that relate to referent clock excitation $f_{ref} = 80$ MHz are given in Fig. 10. The DES-DLL is operatives within the frequency range from 55 MHz up to 166 MHz.

Timing diagrams that correspond to referent input clock pulses, CLK_{ref}, and buffer output, CLK_{out}, are given in Fig. 10a. Fig. 10 shows that the locking time, T_{LOCK}, between the referent CLK_{ref} and output CLK_{out} pulses is less than 200 ns. We define T_{LOCK} as a time interval starting from initial condition up to the instant when total coincidence of rising and falling edges between both pulses, CLK_{ref} and CLK_{out}, exists (see Fig. 10a). If we assume that CLK_{ref} is symmetrical then the coincidence corresponds to 50% duty-cycle of CLK_{out}.

Fig. 10b and c deals with waveforms that are obtained at the outputs UP1 (UP2), DN1 (DN2), and V_{ctrl1} (V_{ctrl2}). As can be seen from Fig. 8(b) (c) UPx and DNx signals define the control voltage V_{ctrlx} during the transition period ($0 < t < T_{LOCK}$). After that the system enters in stable state and UPx and DNx signals disappear and V_{ctrlx} takes a constant value.

According to the obtained results we can conclude that the proposed DES-DLL can be seen to have a wide-operational range and good duty-cycle correction capability.

Simulation results presented in Fig. 11 show that, within the full DLL-DES's operating range (55–166 MHz), the duty cycle error is less then 0.8%.

In Table 2, a comparative survey of pulse width control loop (PWCL) characteristics, available to us from the literature, is given.

Table 2
Comparative survey of PWCL characteristics

References	[8] Mu	[13] Han	[14] Yang	[15] Lin	[16] Tu	DLL-DES
Frequency range	625 MHz	0.5–1.25 GHz	400 MHz	0.3–1 GHz	500 MHz	55–166 MHz
CMOS technology	0.8 μm	0.35 μm	0.35 μm	0.35 μm	0.35 μm	1.2 μm
Locking time	300 ns	310 ns	120 ns	4 μs	1 μs	<200 ns
Duty-cycle error	n.a.	±0.1%	n.a.	n.a.	n.a.	±0.8%
Reference clock	Internal or external	External	External	External	External	External
Duty-cycle correction	30%	(35–75)%	(45–62.5)%	n.a.	(10–90)%	(20–80)%
Single/double edge correction	Single	Single	Single	Single	Single	Double

Compared to the results presented in [8,13–16] we obtain: (a) fast locking time; (b) low duty-cycle error within the full frequency operating range; (c) wide range of duty-cycle correction; and (d) double-edge correction.

6. Conclusion

In this paper a new DLL architecture with clock alignment capability of both leading and trailing edges is described. In essence, the DLL-DES's represents an alternative solution with additional circuit complexity in comparison to the conventional single-edge correction DLL. The DLL-DES's complexity is result of involving two closed loops which operate separately. The first loop is intended for delay regulation of the rising, while the second for delay regulation of the falling pulse edges. In contrast to similar PWCL designs (presented in References [8,13–16] and compared in respect to performance in Table 2) that are implemented in submicron technology, in our proposal for DLL-DES implementation we have used 1.2 μm CMOS technology. During this, a crucial idea of our paper was to point to the architectural details of DLL-DES, but not to its performance. Namely, the clock aligner has been designed specifically to correct precisely the duty-cycle factor in a multistage clock buffer to $(50 \pm 1)\%$ within the operating frequency range from 55 MHz up to 166 MHz. The proposed DLL based clock aligner keeps the same benefits of conventional DLL's such as good absolute stability, fast-response, and low-level output jitter for both (rising and falling) edges. Such circuits can serve in many applications including clock distribution network within the VLSI ICs, high-speed DRAM, and core-to-core interconnects within a system-on-chip designs.

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