A Method for Improvement Stability of a CMOS Voltage Controlled Ring Oscillators

Goran Jovanović[1] and Mile Stojčev[2]

***Abstract* –A CMOS voltage controlled ring oscillator based on N-stage single-ended chain of different inverter types is described in this paper. The proposal is characterized by increased frequency stability ($\Delta f/f$ <2%) in term of power supply voltage variations in respect to standard solutions ($\Delta f/f$ >4%). The presented results are obtained using HSpice simulation and CMOS library model, level 49, for 1.2μm technology.**

***Keywords* –.Voltage controlled oscillator, ring oscillator, CMOS, frequency stability**

I. INTRODUCTION

A voltage controlled oscillator (VCO) is one of the most important basic building blocks in analog and digital circuits [1]-[6]. There are many different implementations of VCOs. One of them is a ring oscillator based VCO, which is commonly used in the clock generation subsystem. The main reason of ring oscillator popularity is a direct consequence of its easy integration. Due to their integrated nature, ring oscillators have become an essential building block in many digital and communication systems. They are used as voltage-controlled oscillators (VCO's) in applications such as clock recovery circuits for serial data communications [1], [2], disk-drive read channels [3], on-chip clock distribution [4], and integrated frequency synthesizers [5], [6]. The design of a ring oscillator involves many tradeoffs in terms of speed, power, area, and application domain. The problem of designing a ring oscillator is in focus of our interest in this paper. This paper proposes a suitable method for increasing frequency stability of a CMOS ring VCO.

The rest of the text is organized as follows. In Section 2, we give a brief review of voltage controlled ring oscillators, and define some crucial operating parameters. Hardware description of the proposed ring oscillator is presented in Section 3. In addition we present the simulation results which relate to frequency stability in terms of temperature and supply voltage variation. In Section 4, we define the terms of jitter and phase noise in ring oscillators, and present the appropriate simulation results. Finally, conclusion is given in Sections 5.

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II. CMOS RING VCO – A REVIEW

A ring oscillator is comprised of a number of delay stages, with the output of the last stage fed back to the input of the first. To achieve oscillation, the ring must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. Each delay stage must provide a phase shift of π/N, where N is the number of delay stages. The remaining π phase shift is provided by a dc inversion [7]. This means that for an oscillator with single-ended delay stages, an odd number of stages are necessary for the dc inversion. If differential delay stages are used, the ring can have an even number of stages if the feedback lines are swapped. Examples of these two circuits are shown in Fig. 1.

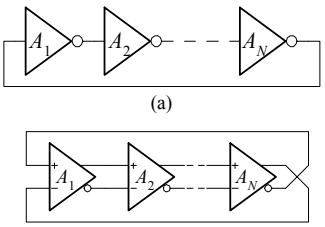

Fig. 1. Ring oscillator types: (a) single-ended and (b) differential

In order to determine a frequency of the ring oscillator we will use its linear model as is given in Fig. 2.

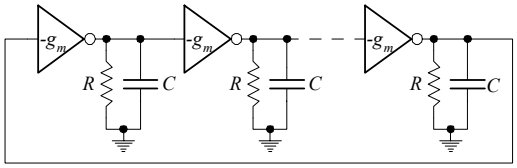

Fig. 2. Linear model of ring oscillators

We assume that all inverting stages are identical and that they can be modeled as a trans-conductance loaded by a parallel connection of resistor R and capacitor C. The gain of the inverting stage is defined as

$$A_1(j\omega) = A_2(j\omega) = ... = A_N(j\omega) = \frac{-g_m R}{1 + j\omega RC} \qquad (1)$$

According to Barkhausen criteria the ring oscillator is operative when the following conditions are satisfied

$$\left|A_1(j\omega) \cdot A_2(j\omega) \cdot ... \cdot A_N(j\omega)\right| = 1 \text{, and}$$

$$\angle A(j\omega) = \theta = \arctan \omega RC = \frac{2k\pi}{N}. \quad (2)$$

The frequency of oscillation is given by

$$\omega_0 = \frac{\tan\theta}{RC} \quad (3)$$

and the minimal single stage gain is

$$g_m R \geq \frac{1}{\cos\theta}. \quad (4)$$

Alternatively we can derive an equation for the frequency of oscillation if we assume that each stage provides a delay of t_d. The signal goes through each of the N delay stages once to provide the first π phase shift in a time of $N\ t_d$. Then, the signal must goes through each stage a second time to obtain the remaining π phase shift, resulting in a total period of $2\ N\ t_d$. Therefore, the frequency of oscillation is

$$f_0 = \frac{1}{2Nt_d}. \quad (5)$$

The difficulty in obtaining a value for the frequency arises when trying to determine t_d, mainly due to the nonlinearities and parasitic of the circuit. As is referred in [7] the delay per stage is defined as the change in output voltage at the midpoint of the transition, V_{SW}, divided by the slew rate, I_{ss}/C, resulting in a delay per stage of $C\ V_{SW}/I_{ss}$. Using definition (5), the oscillation frequency is given by

$$f_0 = \frac{I_{ss}}{2NV_{sw}C}. \quad (6)$$

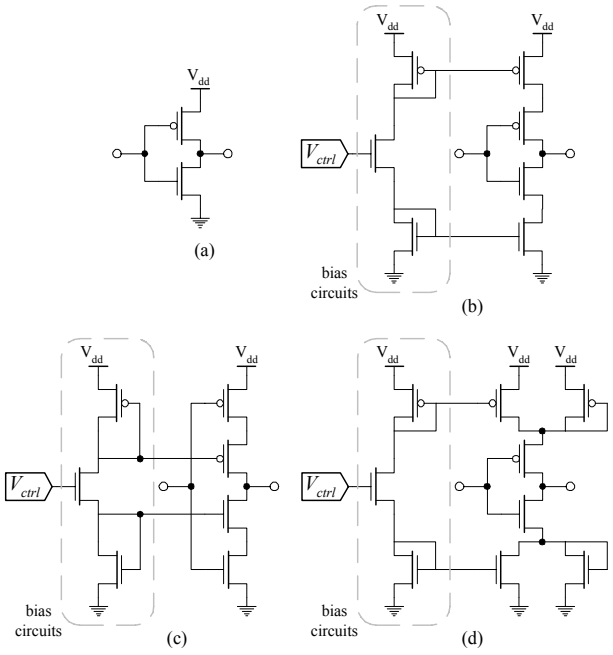

Fig. 3. Invertor: (a) basic type; (b) current starved with output-switching; (c) current starved with power-switching; (d) current starved with symmetrical load;

III. RING OSCILLATOR INVERTING STAGE

As we have already mentioned, the ring oscillators is realized with N inverter stages. There are numerous types of inverter stages by which a ring oscillator can be realized [8], [9]. Some of the standard solutions are pictured in Fig. 3.

Designs given in Fig. 3 b), c), d) are of current starved type, for which the charging and discharging output capacitor current is limited by a bias circuit. |More details related to realization of this type of inverter stage can be found in References [8], [9].

Relative frequency deviations in term of temperature variations for 3-stages ring oscillators based on type of inverters stages presented in Fig. 3 are given in Fig. 4. In general all frequency deviations have similar behavior, but the basic type (Fig. 3a)) and current starved with symmetrical load (Fig. 3d)) inverters have the highest, while current starved with output-switching (Fig. 3b)) inverter has the lowest sensitivity. The ratio of relative frequency deviations between basic type (Fig. 3a)) and current starved with output-switching (Fig. 3b)) inverters is 5:1.

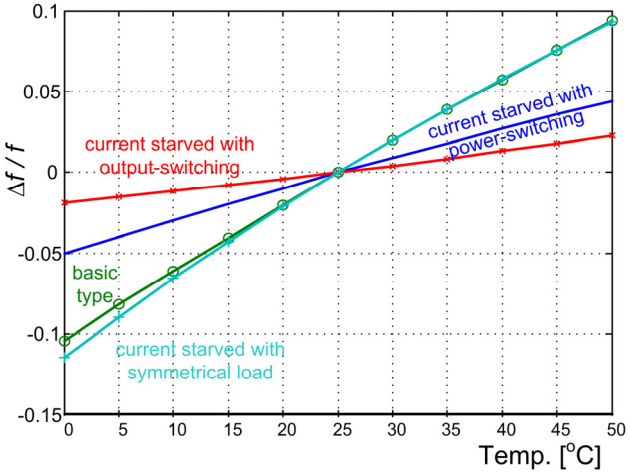

Fig. 4. Relative frequency deviation in term of temperature variation

Relative frequency deviations in term of power voltage supply variations for 3-stages ring oscillators based on type of inverters stages presented in Fig. 3 are given in Fig. 5. As can be seen from Fig 5, the basic type (Fig. 3(a)) and current starved with symmetrical load (Fig. 3(d)) inverters have characteristics with negative slope, while current starved with output-switching (Fig.3(b)) and current starved with power-switching (Fig. 3(c)) inverters have characteristics with positive slope. Absolute value of inverters sensitivity in function to power supply voltage variation is within a range of 10% excluding current starved inverter with power-switching (Fig. 3c)) inverters which has sensitivity of 5%.

Taking into consideration the opposite slope characteristics of the relative frequency deviations in terms of power voltage supply variations of the mentioned inverters (Fig. 5), we can conclude that is reasonable to design a ring oscillator composed of cascade chain of inverters. For example, odd numbered inverters can have positive, while even numbered negative slope. In this way, the relative

frequency deviation in term of power voltage supply can be drastically reduced (more than 100%).

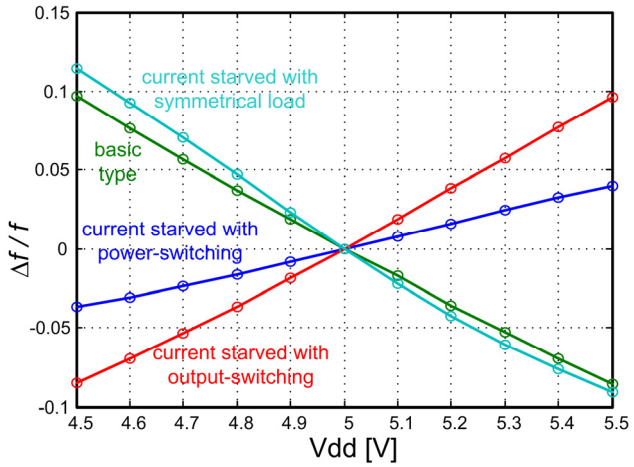

Fig. 5. Relative frequency deviation in term of power supply voltage variation

Several typical design solutions of 3-, 5- and 7- stages ring oscillators with reduced sensitivity are given in Fig. 6. a), b) and c), respectively. We call them as combined ring oscillators. Let note that in combined ring oscillators the odd numbered inverter stages are implemented with basic type, while even numbered as current starved with output-switching inverters.

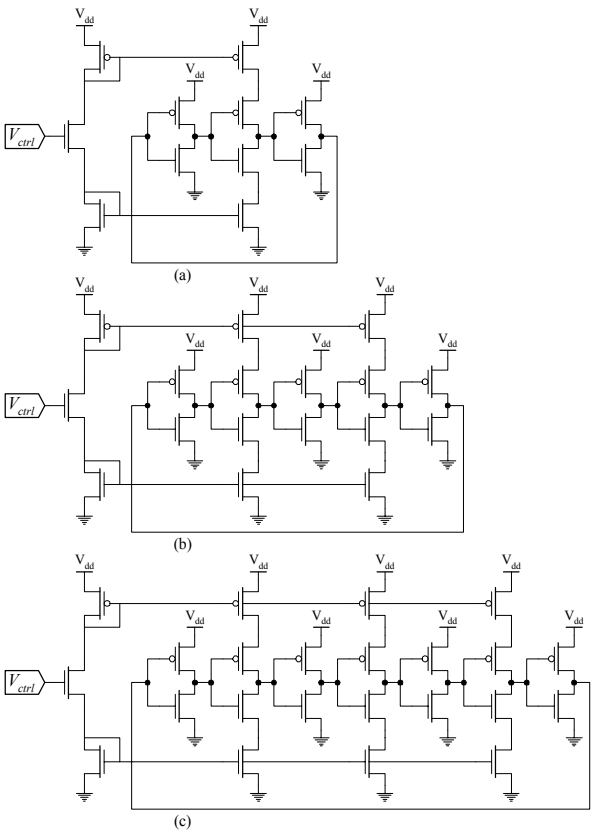

Fig. 6. Combined ring VCOs

The relative frequency deviations in term of power supply voltage for all three type of ring oscillators pictured in Fig. 6 are given in Fig. 7. By analyzing the results presented in Fig. 7 we can conclude the following: The relative sensitivity of the ring oscillator from Fig. 6 a) is less than 2%, while for those given in Fig. 6 b) and c) is less than 1%.

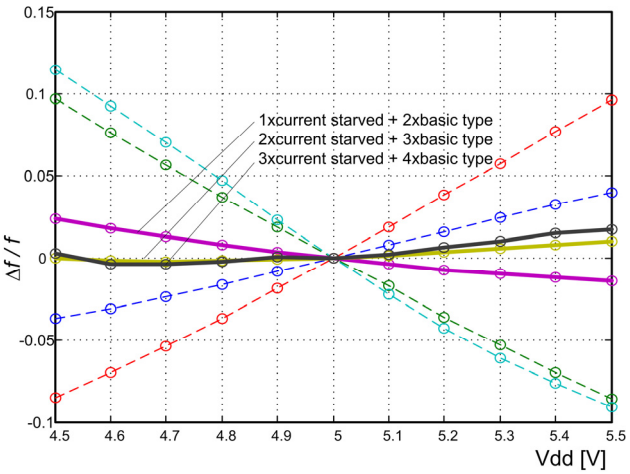

Fig. 7. Relative frequency deviation in term of power supply voltage variation for proposed ring VCOs

IV. JITTER AND PHASE NOISE IN RING OSCILLATORS

In general, CMOS circuits are sensitive both to power supply and temperature variations, as well as to noise generated in IC's building blocks (noise is inserted through power supply and the substrate). Due to these effects, the propagation delay, t_d, is variable [10], [11], [12]. As a consequence there are variations in t_d, in respect to its nominal value. This deviation is manifested as variation of the rising and falling pulse edges, and is referred as jitter (see Fig. 8).

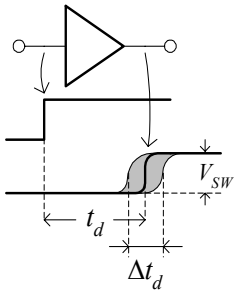

Fig. 8. Jitter effect

As can be seen from Fig. 8 the jitter for the rising edge is defined as a rms time error value, $\overline{\Delta t_d}^2$. The normalized jitter value is defined as a ratio between the effective time error and its nominal delay value, i.e. $\frac{\Delta t_{d\ rms}}{t_d}$.

Consider now a VCO with nominal period T_0, and with a timing error accompanying each period that is Gaussian, with

zero mean and variance $\overline{\Delta t_{VCO}}^2$. If this timing error is expressed in terms of phase, $\Delta\phi=2\pi\Delta t/T_0$, then the variance of the phase error per cycle of oscillation is given by [10]

$$\sigma_\phi^2 = (2\pi)^2\left(\frac{\Delta t_{VCO\ rms}}{T_0}\right)^2. \quad (7)$$

The phase noise power spectral density expressed in terms of frequency is given by [10]

$$S_\phi(f) = \frac{f_0}{f^2}\left(\frac{\Delta t_{VCO\ rms}}{T_0}\right)^2. \quad (8)$$

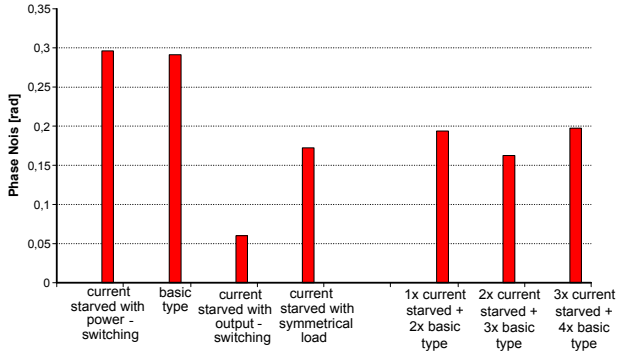

Fig. 9. Relative frequency deviation in term of power supply voltage variation for proposed ring VCOs

The amount of phase noise for all types of ring oscillators discussed in this paper is sketched in Fig. 9. By analyzing Fig. 9 we can conclude that the best performance (phase noise approx. 0.06 rad) have ring oscillators based on current starved inverters with output-switching, while the worst (phase noise approx. 0.3 rad) correspond to ring oscillators realized with basic type or current starved with power-switching inverters. Combined ring oscillators, composed of basic and current starved with output-switching inverters, have approximately phase noise within the range 0.16-0.2 rad.

V. Conclusion

Ring oscillators are basic building blocks of complex integrated circuits. They are mainly used as clock generating circuits. Many different types of ring oscillators are presented in literature [1]-[4]. They differ in respect to architectural, realization of inverters stages, number of inverter stages, etc. In this paper we have considered realization of ring oscillator based on four different types of single-ended inverters. The simulation was performed using HSpice Version 03.2006 and library model for 1.2µm CMOS technology. According to the obtained simulation results we can conclude:

a) that for frequency stability in terms of temperature variations the best performance ($\Delta f / f$ <2%) has current starved inverters with output-switching;

b) that for frequency stability in terms of power supply voltage variations the best performance ($\Delta f / f$ <4%) has current starved inverters with power-switching;

c) by realizing combined types of ring oscillator the relative frequency deviation in terms of power supply voltage variations can be significantly decreased ($\Delta f / f$ <2%) in respect to the best standard solutions ($\Delta f / f$ >4%).

d) in respect to phase noise, ring oscillators based on current starved inverters with output-switching have the best performance (phase noise approx. 0.06 rad).

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